PN531/C2

Near Field Communication (NFC) controller

Rev. 3.0 — 10 February 2006 Draft Product data sheet

1. General description

The PN531 is a highly integrated transmission module for contactless communication at 13.56 MHz including microcontroller functionality based on an 80C51 core. The transmission module utilises an outstanding modulation and demodulation concept completely integrated for different kinds of passive contactless communication methods and protocols at 13.56 MHz.

The PN531 support 3 different operating modes:

- Reader/writer mode supporting ISO/IEC 14443A / MIFARE® and FeliCa scheme
- Card interface mode supporting ISO/IEC 14443A / MIFARE® and FeliCa scheme
- NFCIP-1 mode

Enabled in reader/writer mode for ISO/IEC 14443A / MIFARE®, the PN531's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A /MIFARE® cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443A / MIFARE® compatible cards and transponders. The digital part handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The PN531 supports MIFARE® Classic (e.g. MIFARE® Standard) products. The PN531 supports contactless communication using MIFARE® Higher Baudrates up to 424 KBaud in both directions.

Enabled in the reader/ writer mode for FeliCa, the PN531 transmission module supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection like CRC. The PN531 supports contactless communication using FeliCa Higher Baudrates up to 424 KBaud in both directions.

Enabled in card mode the PN531 transmission module is able to answer to a reader/writer command either according to FeliCa or ISO/IEC 14443 A / MIFARE® card interface mode. The PN531 generates the digital load-modulated signals and in addition with an external circuit the answers can be send back to the reader/writer. A complete card functionality is only possible in combination with a secure memory IC.

Additionally, the PN531 transmission module offers the possibility to communicate directly to a second NFCIP-1 device in the NFCIP-1 mode. The NFCIP-1 mode offers different communication transfer speeds up to 424kbit/s according to the ECMA 340 NFCIP-1 ISO/IEC 1892 standards. The digital part handles the complete NFCIP-1 framing and error detection.

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Transfer speeds on the RF interface above 424kbit/s are supported by the digital part of the PN531 module. The modulation to transmit and the demodulation to receive data at transfer speeds has than to be done by an external circuit.

To make information exchange to the host systems several interfaces are implemented:

- USB 2.0 full speed interface
- SPI interface
- I^2C interface
- Serial UART (similar to RS232 with 0 and PVDD voltage levels)

2. Features

- 80C51 microcontroller core with 32 kB ROM and 1 kB RAM
- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF Level detector
- Integrated data mode detector
- Supports ISO/IEC 14443A/MIFARE®
- Typical operating distance in reader/writer mode for communication to a ISO/IEC 14443A/MIFARE® or FeliCa card up to 5 cm depending on the antenna size and tuning
- Typical operating distance in NFCIP-1 mode up to 5 cm depending on the antenna size and tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE® card or FeliCa card interface mode of about 7 cm depending on the antenna size and tuning and the external field strength
- Supports MIFARE® Classic encryption in reader/writer mode and MIFARE® higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Supports contactless communication according to the FeliCa scheme at 212 KBaud and 424 KBaud
- Integrated RF interface for NFCIP-1 up to 424 KBaud
- Supported host interfaces
  - USB 2.0 full speed interface
  - SPI interface
  - I^2C interface
  - High Speed Serial UART (similar to RS232 with 0 and PVDD voltage levels)
- Flexible interrupt using IRQ pin
- Hard reset with low power function
- Power-down mode per embedded firmware
- Programmable timer
- Internal oscillator to connect 27.12 MHz crystal
- Internal oscillator to connect a 4 MHz crystal for the USB interface
- 3.3 V power supply when not USB bus powered
- USB bus powered possibility
- Power Switch for external secure component
- Specific IO ports for external devices control

3. Applications

- Mobile and portable devices
- PC world
- Consumer application

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BUS}	USB Supply Voltage (USB mode)			4.2	5	5.25	V
	Supply Voltage (non USB mode)	$V_{BUS} = DV_{DD}$; $V_{SS} = 0$ V		2.5	3.3	3.6	V
TV_{DD}, AV_{DD}, DV_{DD}	Supply Voltage	$TV_{DD} = AV_{DD} = DV_{DD}$ $V_{SS} = 0$ V	[1]	2.5	3.3	3.6	V
PV_{DD}	Supply Voltage for host interface	$V_{SS} = 0$ V		1.6		3.6	V
SV_{DD}	Output Voltage for SAM interface	$V_{SS} = 0$ V (SV_{DD} Switch Enabled)		DV_{DD} -1.0	3.3	DV_{DD}	V
IV_{BUS}	Maximum load current (USB mode)	measured on V_{BUS}				150	mA
	Maximum Inrush current limitation	At power up (curlimoff =0)				100	mA
I_{HPD}	Hard Power-down Current (not powered from USB)	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD}$ =3 V, RF level detector off				10	µA
I_{SPD}	Soft Power-down Current (not powered from USB)	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD}$ =3 V, RF level detector on				30	µA
$I_{suspend}$	USB suspend Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD}$ =3 V, RF level detector on (without resistor on D+/D-)				250	µA
I_{DVDD}	Digital Supply Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD}$ =3 V, RF level detector on, SV_{DD} switch off	[1]		15		mA
I_{SVDD}	SV_{DD} Load Current	2.7 < DV_{DD}, 3.6 > DV_{DD}, SV_{DD} switch On				30	mA
I_{AVDD}	Analog Supply Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD}$ =3 V, RF level detector on			6		mA
I_{TVDD}	Transmitter Supply Current	During RF Transmission, TV_{DD} = 3 V			60	100	mA
P_{totusb}	continuous total power dissipation in USB mode	T_{amb} = -30 to +85 °C				0.55	W
P_{tot}	continuous total power dissipation in non USB mode	T_{amb} = -30 to +85 °C				0.15	W
T_{amb}	operating ambient temperature			-30		+85	°C

[1] DVDD, AVDD and TVDD shall always be at the same supply voltage.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PN5310A3HN/2xx [1]	HVQFN40	plastic, heatsink very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

[1] xx is the reference of the ROM code version.

6. Marking

Table 3: Marking codes

Line	Marking	Description
5310_xx [1]		

[1] xx is the reference of the ROM code version

7. Block diagram

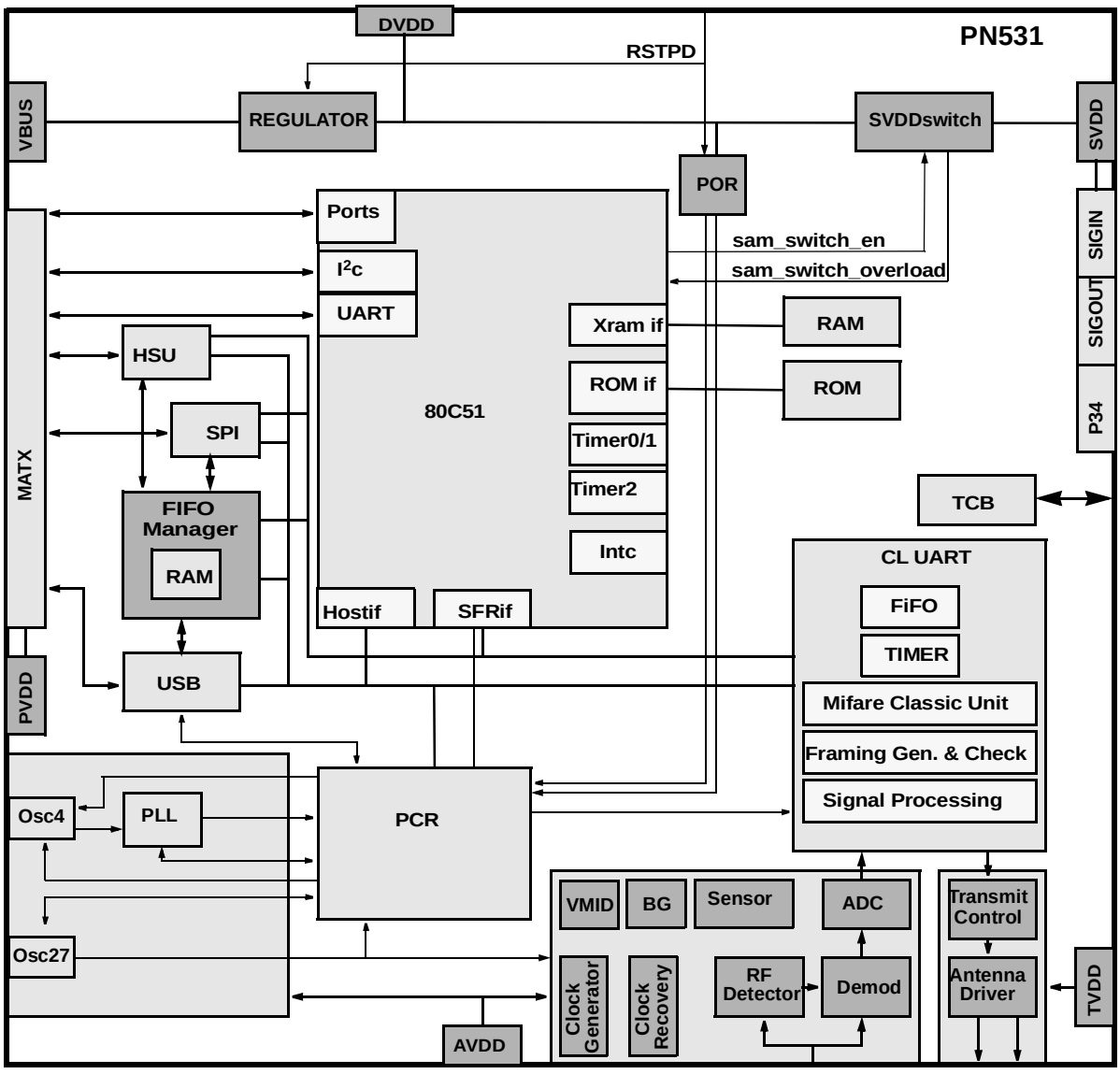


Fig 1. Block diagram of PN531

8. Pinning information

8.1 Pin description

Table 4: PN531 Pin description

Symbol	Pin	Type	Pad Ref Voltage	Description
DVSS	1	PWR		Digital Ground
LOADMOD	2	O	DVDD	Load Modulation output provides digital signal for FeliCa and MIFARE® card operating mode
TVSS1	3	PWR		Transmitter Ground: supplies the output stage of TX1 and TX2
TX1	4	O	TVDD	Transmitter 1: delivers the modulated 13.56 MHz energy carrier
TVDD	5	PWR		Transmitter power supply: supplies the output stage of TX1 and TX2
TX2	6	O	TVDD	Transmitter 2: delivers the modulated 13.56 MHz energy carrier
TVSS2	7	PWR		Transmitter Ground: supplies the output stage of TX1 and TX2
AVDD	8	PWR		Analog Power Supply
VMID	9	PWR	AVDD	Internal Reference Voltage: This pin delivers the internal reference voltage.
RX	10	I	AVDD	Receiver Input: Input pin for the reception signal, which is the load modulated 13.56 MHz energy carrier from the antenna circuit.
AVSS	11	PWR		Analog Ground
AUX1	12	O	DVDD	Auxiliary Output: This pin delivers analog and digital test signals.
AUX2	13	O	DVDD	Auxiliary Output: This pin delivers analog and digital test signals.
OSCIN	14	I	AVDD	Crystal Oscillator Input: input to the inverting amplifier of the oscillator.This pin is also the input for an externally generated clock (fosc = 27.12 MHz). In test mode this signal is used as test clock input
OSCOUT	15	O	AVDD	Crystal Oscillator output: Output of the inverting amplifier of the oscillator.
I0	16	I	DVDD	Interface mode lines: selects the used host interface (refer to Table 69 “Config IO_I1 (6103h)” for details). In test mode I0 is used as test signals.
I1	17	I	DVDD	Interface mode lines: selects the used host interface (refer to Table 69 “Config IO_I1 (6103h)” for details). In test mode I0 is used as test signals.
TESTEN	18	I	DVDD	Test enable pin: When set to 1 enable the test mode. When set to 0 reset the TCB and disable the access to the test mode.
OSC2OUT	19	O	DVDD	Crystal Oscillator output: Output of the inverting amplifier of the oscillator for the USB clock.
OSC2IN	20	I	DVDD	Crystal Oscillator Input: input to the inverting amplifier of the oscillator for the USB clock generation. This pin is also the input for an externally generated clock (fosc =4 MHz).
P35	21	IO	DVDD	General purpose IO signal
P34	22	IO	SVDD	General purpose IO signal or CLK signal for the SAM
SIGOUT	23	O	SVDD	Contactless communication interface output: delivers a serial data stream according to NFCIP-1 and output signal for the SAM. In test mode this signal is used as test signal output.
SIGIN	24	I	SVDD	Contactless communication interface input: accepts a digital, serial data stream according to NFCIP-1 and input signal from the SAM. In test mode this signal is used as test signal input.

Table 4: PN531 Pin description *...continued*

Symbol	Pin	Type	Pad Ref Voltage	Description
SVDD	25	IO		Output power for SAM power supply. Switched on by Firmware with an overload detection. Used as a reference voltage for SAM communication.
P31	26	IO	PVDD	General purpose IO signal.Can be configured to act either as TX line of the second serial interface or general purpose IO. In test mode this signal is used as input and output test signal.
P30	27	IO	PVDD	General purpose IO signal. Can be configured to act either as RX line of the second serial interface or general purpose IO. In test mode this signal is used as input and output test signal.
IRQ	28	O	PVDD	Interrupt request: Output to signal an interrupt event to the host
RSTOUT	29	IO	PVDD	Output reset signal. When Low it indicates that the circuit is in reset state.
DELATT	30	O	PVDD	Optional output for an external 1.5 KΩ resistor connection on D+.
NSS	31	IO	PVDD	Not Slave Select (refer to Table 81 “HOST interface selection” for details). In test mode this signal is used as input and output test signal.
MOSI	32	IO	PVDD	Master Out Slave In (refer to Table 81 “HOST interface selection” for details). In test mode this signal is used as input and output test signal
MISO	33	IO	PVDD	Master In Slave Out (refer to Table 81 “HOST interface selection” for details). In test mode this signal is used as input and output test signal
SCK	34	IO	PVDD	Serial interface clock (refer to Table 81 “HOST interface selection” for details). In test mode this signal is used as input and output test signal
PVDD	35	PWR		Pad power supply
P33_INT1	36	IO	PVDD	General purpose IO signal. Can be used to generate an HZ state on the output of the selected interface for the Host communication and to enter PN531 into Power-down mode without resetting the internal state of PN531. In test mode this signal is used as input and output test signal.
P32_INT0	37	IO	PVDD	General purpose IO signal. Can also be used as an interrupt source In test mode this signal is used as input and output test signal.
RSTPD	38	I	PVDD	Reset and Power Down: When High, internal current sources are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
DVDD	39	PWR		Digital Power Supply
VBUS	40	PWR		USB power supply.

9. Functional description

9.1 Power Distribution

This chapter defines the power distribution scheme according to the different system configuration. The PN531 can be supplied by the USB connector on VBUS or directly on the AVDD, DVDD, PVDD and TVDD. Regarding the system configuration (USB BUS powered or HOST powered), the power distribution shall be different.

9.1.1 USB bus Powered

The power distribution is performed from the USB bus. The power delivered to the different peripherals is controlled by the PN531 chip. The Figure 2 “USB bus powered” on page 8 depicts the system approach for the power distribution. When PN531 is supplied by the USB connector (USB powered) an internal regulator generates the supply voltage for all the parts, and during the power-up phase the inrush current is limited to 100mA.

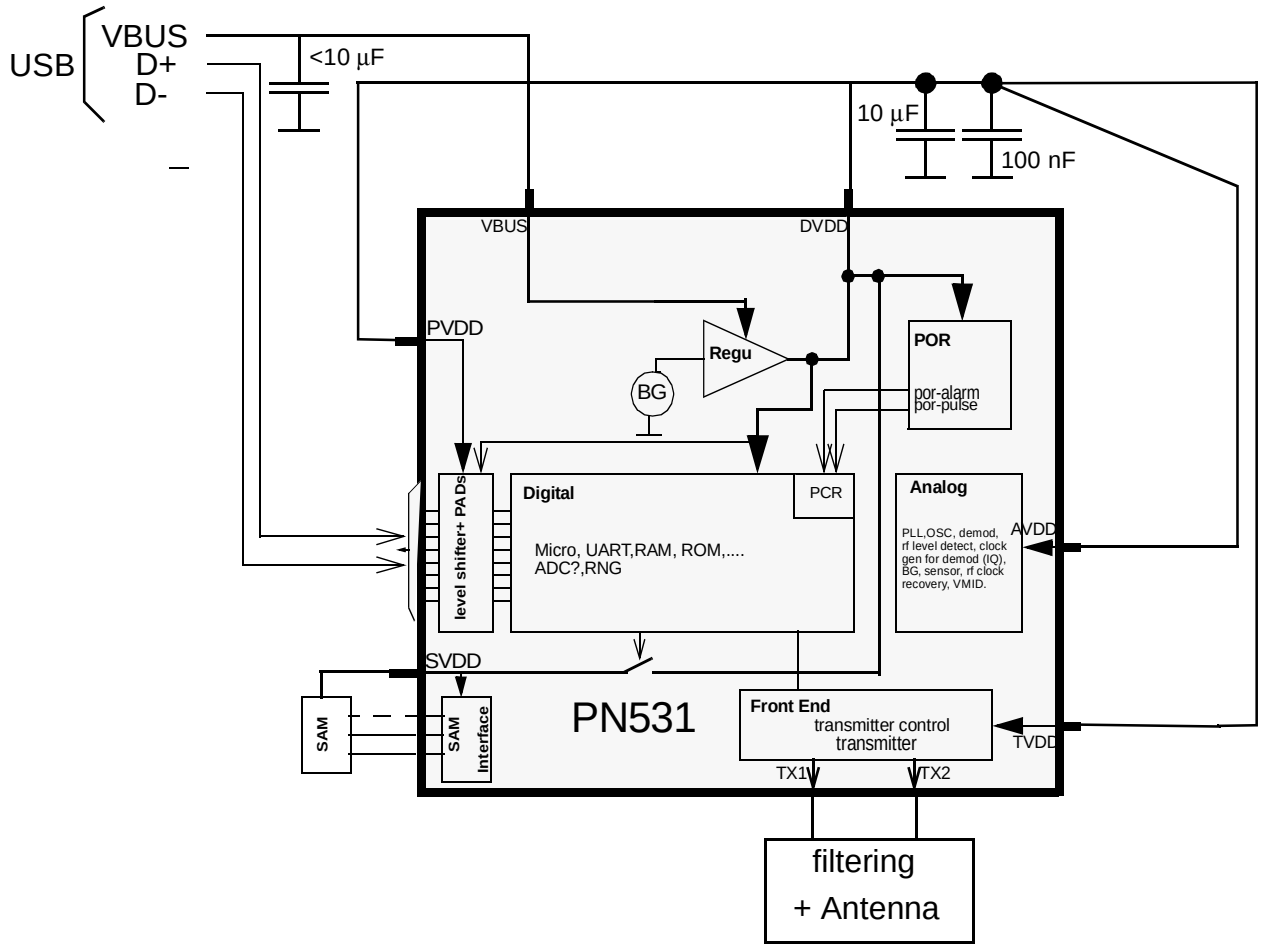


Fig 2. USB bus powered

9.1.2 HOST powered (Single source)

In that case, the power distribution is performed from a single power supply source. The Figure 3 “HOST powered from single source” on page 9 depicts the system approach for the power distribution.

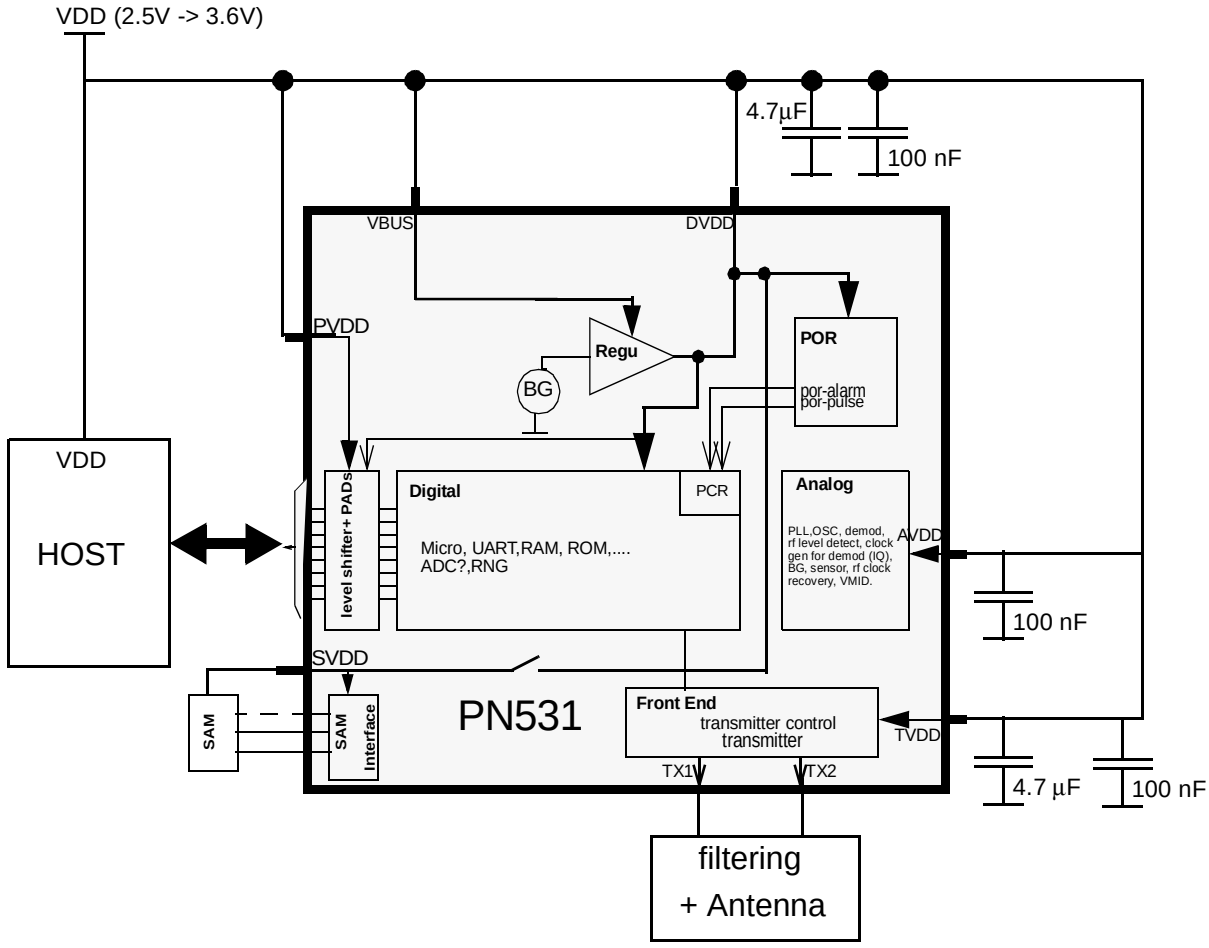


Fig 3. HOST powered from single source

9.1.3 HOST powered (Double source)

The power distribution is performed from the second source from the Host. The Figure 4 “HOST powered from double source” on page 10 depicts the system approach for the power distribution.

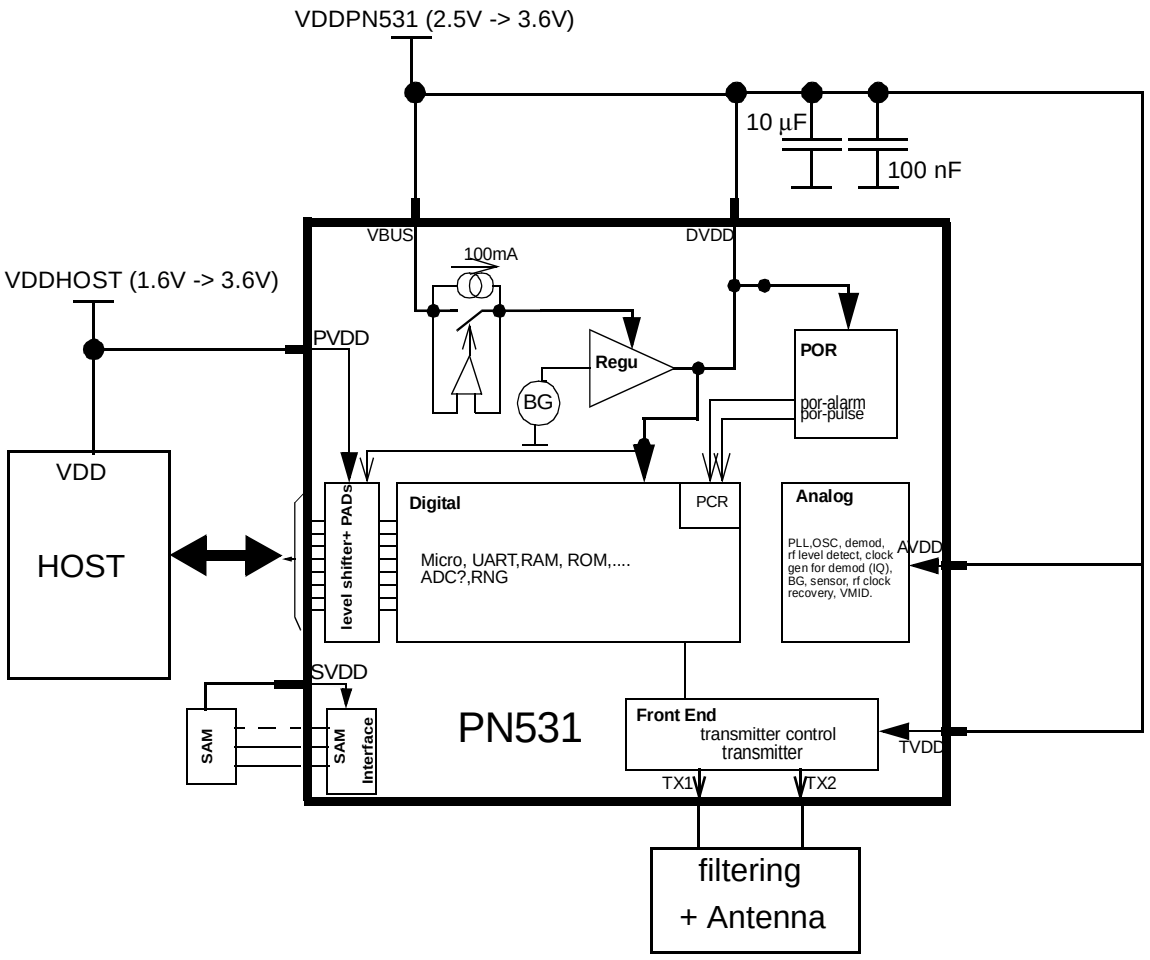


Fig 4. HOST powered from double source

9.1.4 Low power modes

There are 2 different low power modes.

“Hard power-down” controlled by the pin RSTPD. In that case, the PN531 enters into the reset state and the maximum consumption depends on the connection of PN531 to the USB bus or not.

“Soft power-down” controlled by a register. In that case, the PN531 enters into the idle state and the maximum consumption depends if PN531 is “USB powered” or not and if the RF detector is active or not. In that mode the PN531 can be waken up on external events.

Table 5: Current consumption in power-down

Low power mode	Power supply source	Maximum currentconsumption
Suspend	Powered from USB	200 µA (without resistors on D+ / D-)
Suspend with RF detector active	Powered from USB	250 µA (without resistors on D+ / D-)
hard power-down	Not powered from USB	10 µA
soft power-down	Not powered from USB	25 µA
soft power-down with RF detector active	Not powered from USB	30 µA

9.1.5 Power-On Reset

The Power On Reset (POR) module generates the reset signals for the different parts of PN531.

The Power On Reset module is used to control the power-up, power-down and reset phase of PN531.

On the rising edge of the VDD, a POR_PULSE signal is generated to reset the internal registers of PN531. As soon as, VDD reaches 2.4 Volts, The POR_PULSE is deasserted and the system startup phase starts under control of the PCR. The POR-ALARM is internally delayed.

When the RSTPD is asserted, the POR_PULSE and the POR_ALARM are also asserted and all internal current source are cut.

When the power supply voltage drops, the POR asserts the POR_ALARM and the POR_PULSE. The figure hereafter depicts the internal behaviour of POR_PULSE and POR_ALARM for the startup sequence.

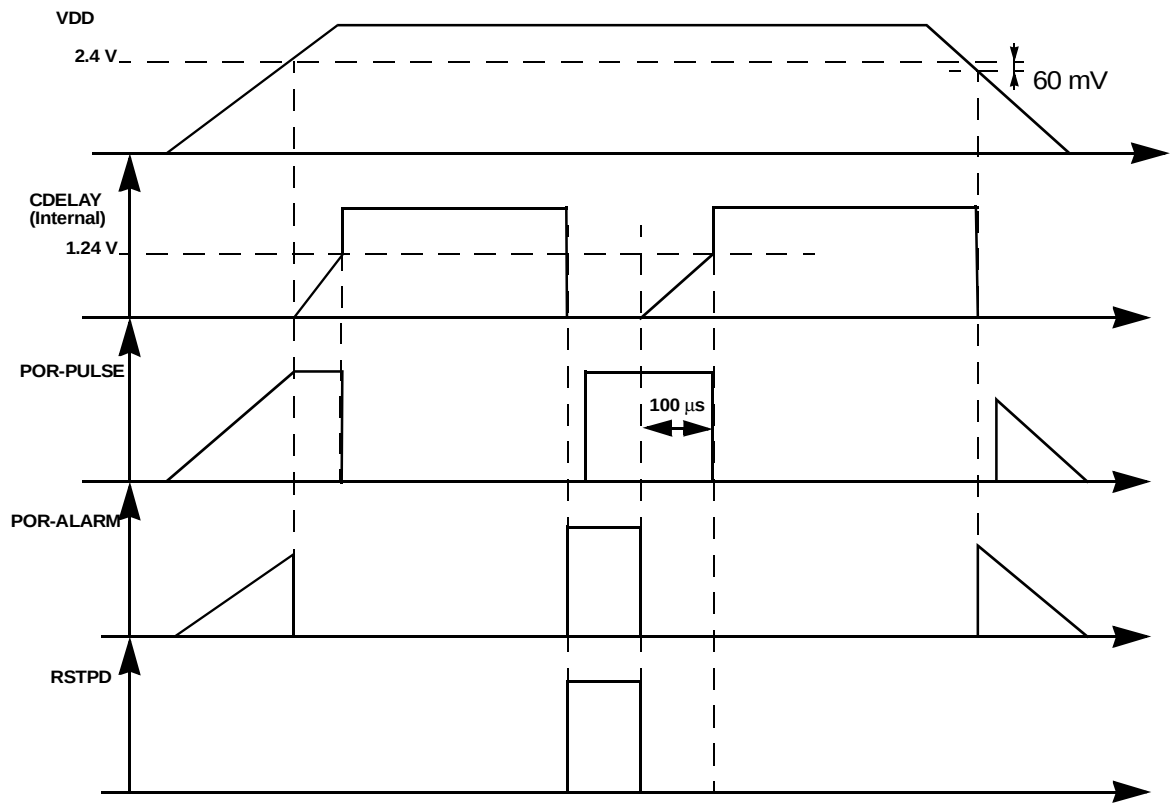


Fig 5. POR Timing diagram

9.1.6 Regulator - short description

The regulator is used to reduce the VBUS voltage to the typical voltage rating of PN531.

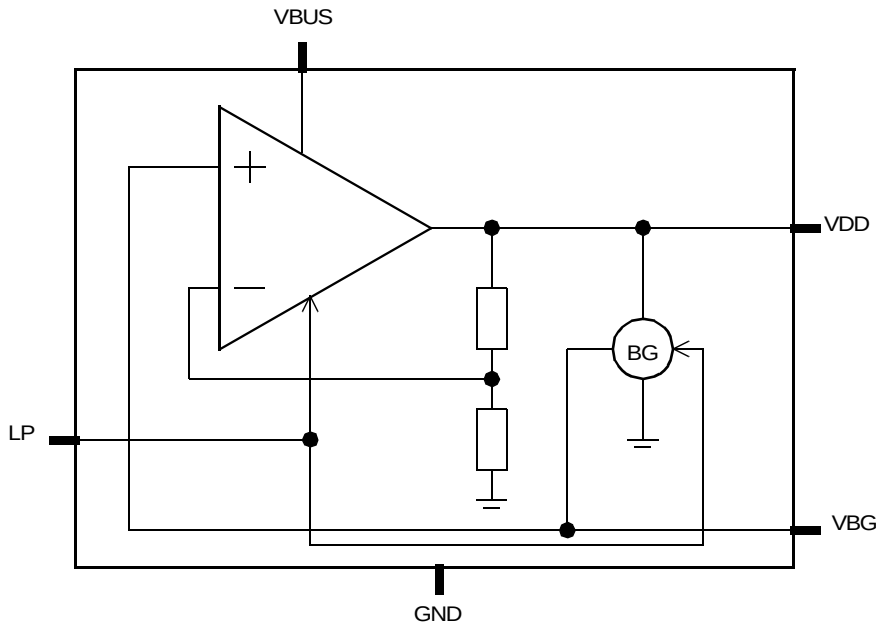


Fig 6. 3.3 V regulator Block diagram.

The 3.3 V regulator is a linear regulator with resistive feed-back. The regulator use the Band-gap for reference voltage. It limits the inrush current during the power-up. The current limitation is disabled through the bit curlimoff.

9.1.7 SVDD switch

The SVDD switch is used to deliver power to the SAM. The SAM switch is enabled by firmware and integrate a current limitation function. The current limitation is not activated when the current is less than 30 mA (Table 72 “Control_rngpower (6106h)” on page 62).

9.2 27.12 MHz XTAL Oscillator

The 27.12 MHz clock applied to the PN531 acts as time basis for the microcontroller, the coder and decoder of the contactless synchronous system. Therefore stability of the clock frequency is an important factor for proper performance. To obtain highest performance, clock jitter has to be as small as possible. This is best achieved by using the internal oscillator buffer with the recommended circuitry. If an external clock source is used, the clock signal has to be applied to pin OSCIN. In this case special care for clock duty cycle and clock jitter is needed and the clock quality has to be verified.

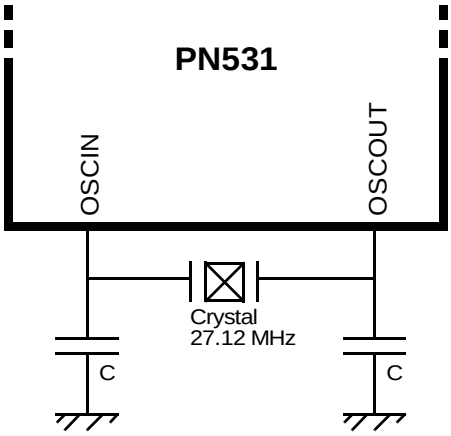


Fig 7. 27.12 MHz Quart connection

9.3 4 MHz XTAL Oscillator

The 4 MHz clock applied to the PN531 is only needed for the USB communication. When the USB interface is not used the 4 MHz quartz oscillator can be suppressed. The enabling of the 4 MHz is under firmware control (Table 14 “PCR Control (6203h)” on page 29).

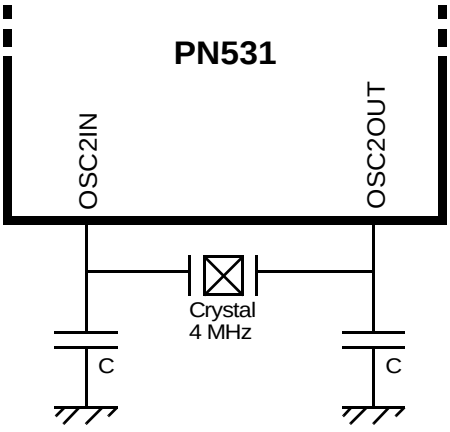


Fig 8. 4 MHz Quartz connection

9.4 Power Clock and Reset Controller

The PCR controller is the controller for the clock generation, the power management and the reset architecture for PN531.

9.4.1 PCR in the system

This block diagram Figure 9 “PN531 Power Management Block diagram” on page 15 shows the relation between the PCR and the onchip blocks.

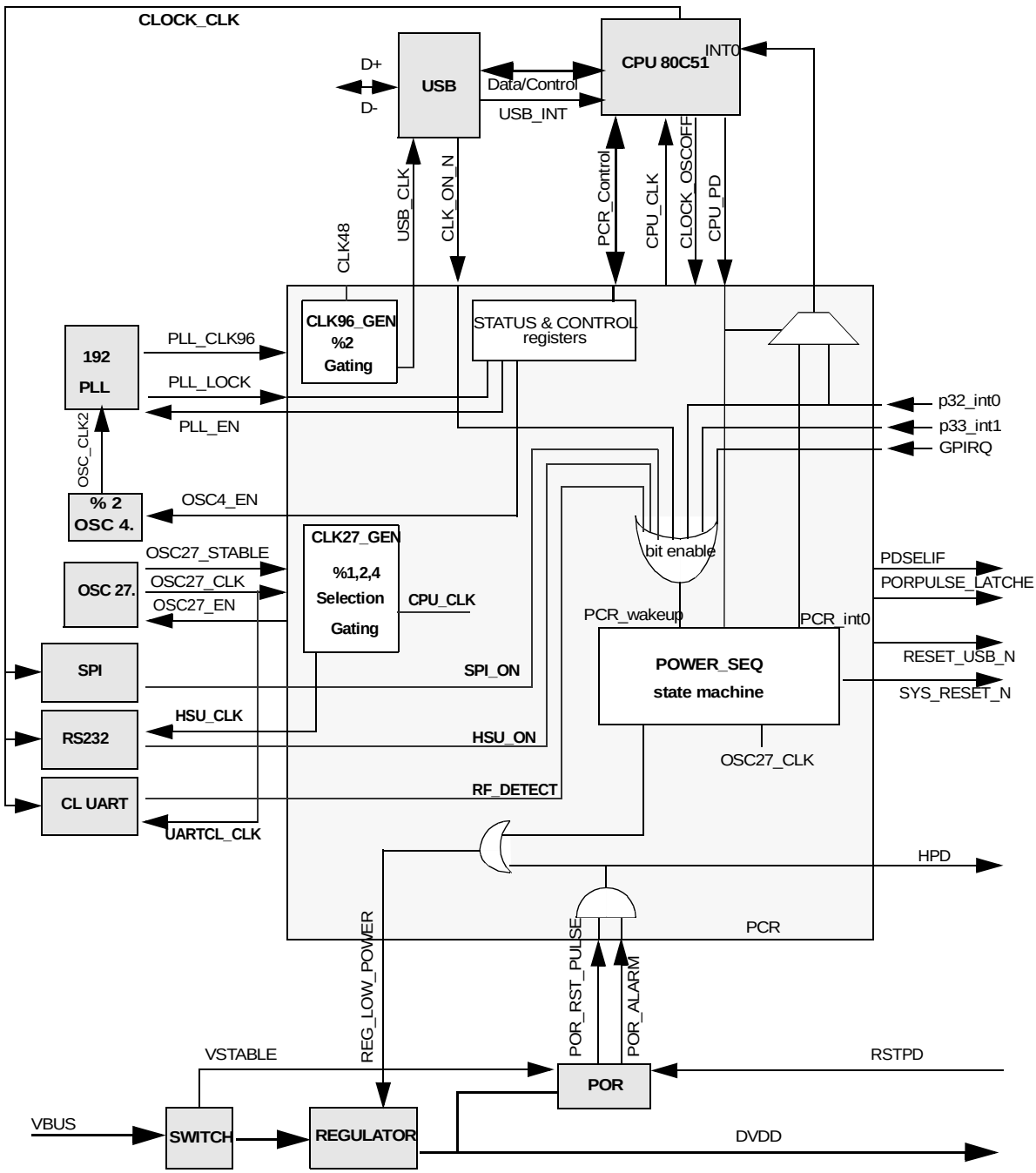


Fig 9. PN531 Power Management Block diagram

Table 6: PN531 Clock source characteristics

Clock name	Frequency MHz	Tolerance	Clock source	Comments
OSC_CLK27	27.12	± 7 kHz	OSC 27	Output of OSC 27
OSC_CLK2	2	± 0.05%	OSC 4	Divided by 2 inside OSC4
PLL_CLK96	96	± 0.25%	PLL 192	Output of PLL
USB_CLK	48	± 0.25%	PLL 192	
CPU_CLK	27.12 / 13.56 / 6.78		OSC 27	Default is 6.78 MHz
HSU_CLK	27.12		OSC 27	

9.4.2 Reset Distribution overview

The SYS_RESET_N signal is the reset that is distributed to the system. SYS_RESET_N is active low. There are three possible resets:

- Power On Reset

  When the circuit is powered up or when there is a voltage drop, POR_RST_PULSE is asserted. SYS_RESET_N is asserted asynchronously with POR_RST_PULSE. SYS_RESET_N is deasserted 30 cycles of 27.12 MHz clock after the system clocks are enabled. SYS_RESET_N is deasserted synchronously on a falling edge of 27 MHz clock. The RSTOUT pin is internally connected to SYS_RESET_N.

- External reset

  The system can order a reset when asserting the RSTPD signal. This signal goes to the analog POR block and creates a POR_RST_PULSE as if the system is being powered.

- Embedded firmware reset

  Software can order a reset when writing a soft_reset bit in the PCR control register Status. SYS_RESET_N is asserted asynchronously with this bit. In that case, the 27.12 MHz clock will not be stopped.

9.4.3 Power management

The power management of the system is divided into hardware and embedded firmware. The power management of the 27 MHz system is done in the power sequencer hardware block, and the power management of the 4 MHz system is done by embedded firmware.

9.4.4 Power Up sequence

The Figure 10 “Power Up sequence in a USB application” on page 18 enclosed here after despicts the power up sequence when the device is USB bus powered.

When VBUS is rising the regulator and the POR starts running.

POR_RST_PULSE is asserted when DVDD rises and is deasserted when DVDD reaches 2.4 V (supervisor threshold). as soon as POR_RST_PULSE is asserted, SYS_RESET_N is asserted and stays asserted until the completion of the power-up and reset sequence.

POR_ALARM is asserted when DVDD rises but is deasserted when the voltage of the internal capacitance C delay is equal to BG_POR (1.2V) The value of the capacitance fixes the T1 delay in the timing diagram.

OSC27_EN is asserted when POR_RST_PULSE is high and POR_ALARM is low, then the 27 MHz oscillator is started. After a time T2 which is analog, the 27 MHz oscillator is stable. When Osc27_stable is asserted, a counter starts counting rising edges of the OSC_CLK27 clock up to 1536. This 1536 value defines the T3 delay in the timing diagram. Then the 27 MHz clocks are generated when the CLOCKS27_ON signal is asserted.

Once the clocks are generated, a counter counts 30 edges of Oscillator 27 MHz clock before deasserting the SYS_RESET_N signal. These 30 cycles of OSC_CLK27 represent the T4 timing in the diagrams. Then the system reset SYS_RESET_N is deasserted.

In a USB application (refer to Figure 10 “Power Up sequence in a USB application” on page 18), the embedded firmware shall start the 4 MHz oscillator. After a timing controlled by embedded firmware (T5 in USB application diagram) which guaranty that the oscillator is stable, the embedded firmware shall start the PLL. Embedded firmware shall poll the PLL_lock signal to enable the 96 MHz clock. This defines the T6 timing in the USB application diagram. When the 96 MHz clock is enabled, the 48 MHz clock exists, embedded firmware shall also enable USB clock by setting USB_enable (refer to Table 10 “PCR Clock Enable Register (6201h)” on page 28)to 1.

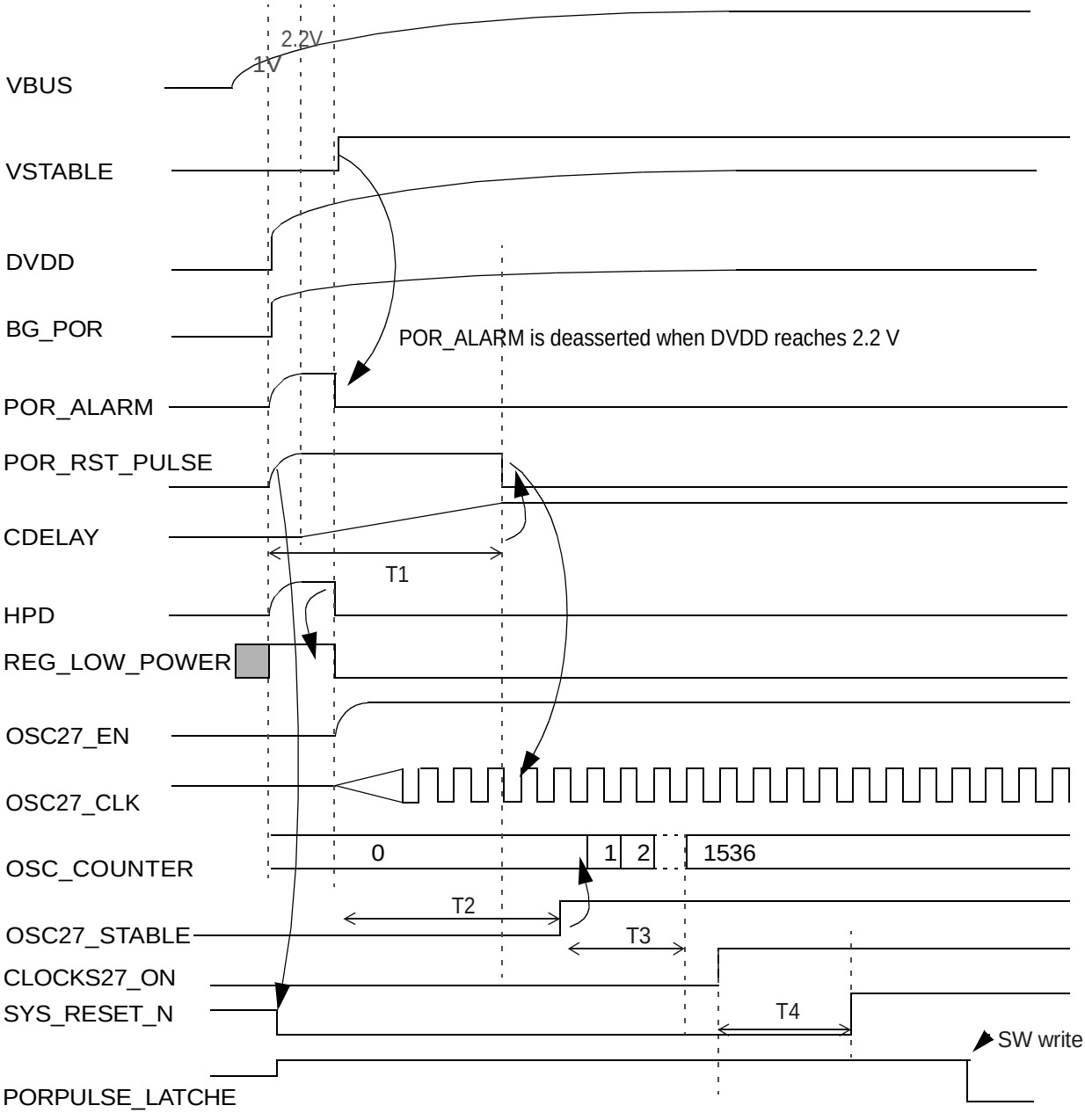


Fig 10. Power Up sequence in a USB application

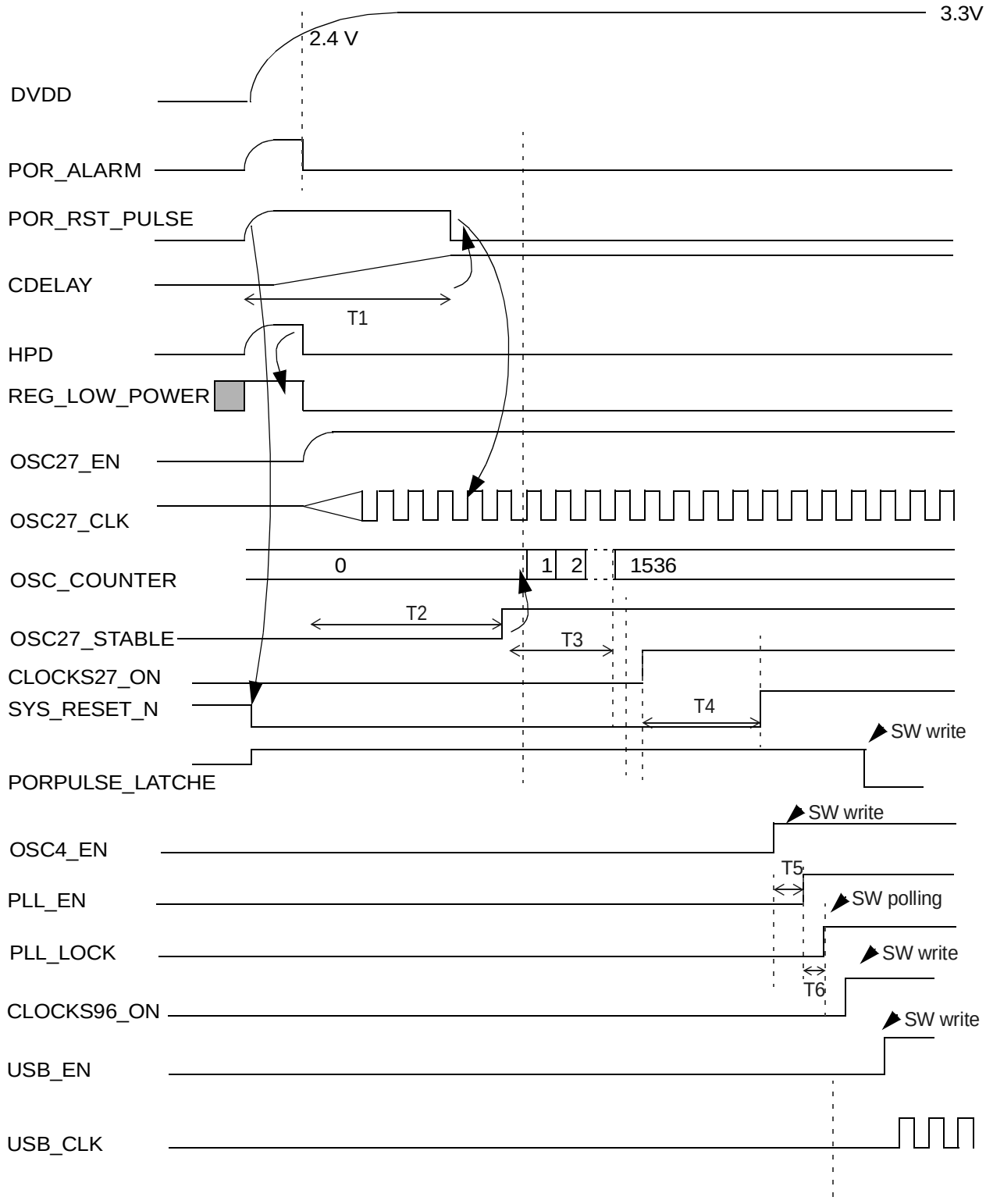


Fig 11. Power Up sequence in a non USB application

9.4.5 Voltage drop

If a voltage drop occurs, the POR analog bloc will assert first POR_ALARM in order to warn that POR_RST_PULSE is asserted. Then system restarts from the power up sequence.

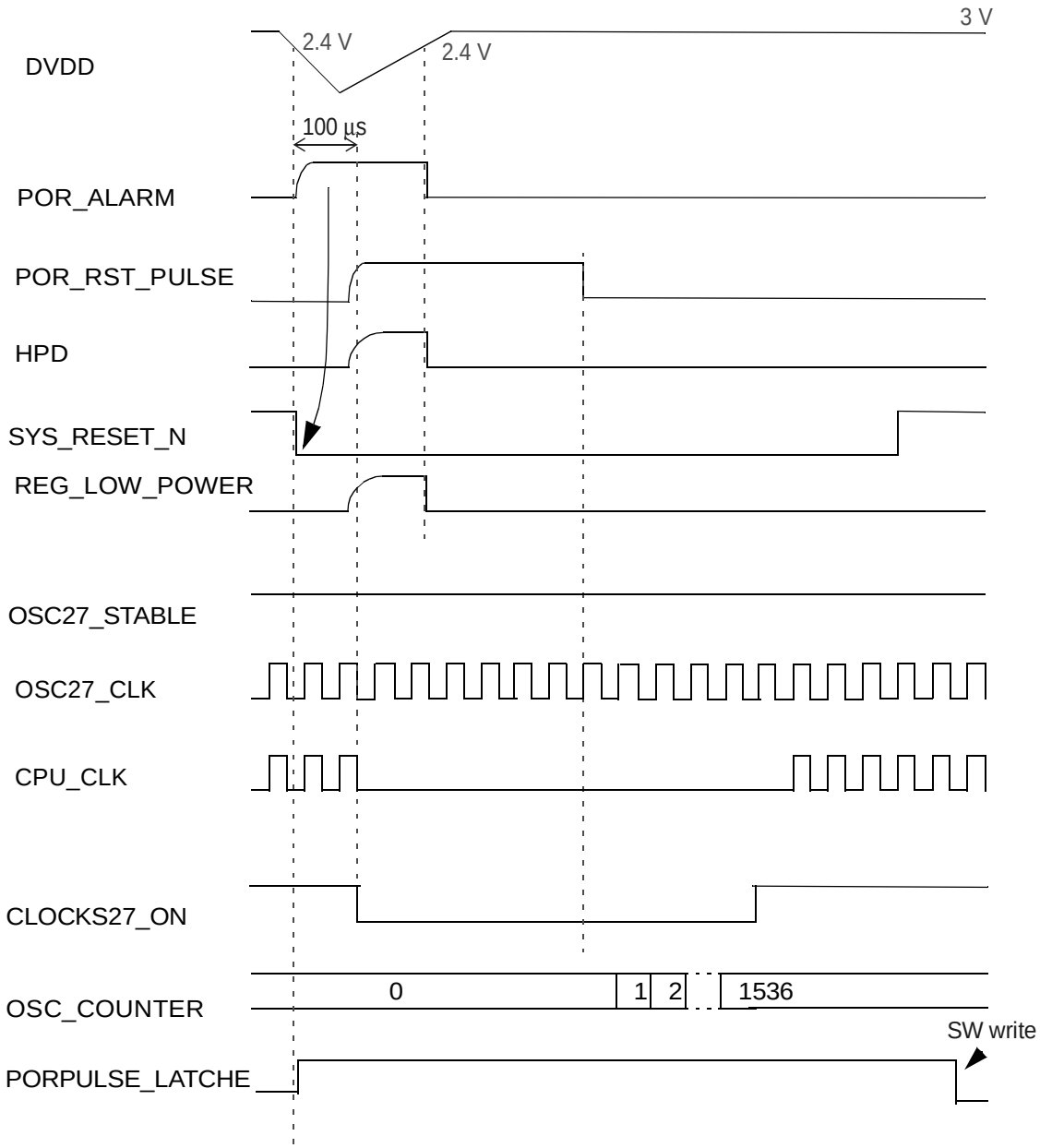


Fig 12. Voltage drop

9.4.6 Shut down mode

When external pin RSTPD is high (active high), both signal POR_ALARM and POR_RST_PULSE are asserted. In this configuration, the system is in hardPower-down mode and the power consumption of the circuit is only due to leakage currents.

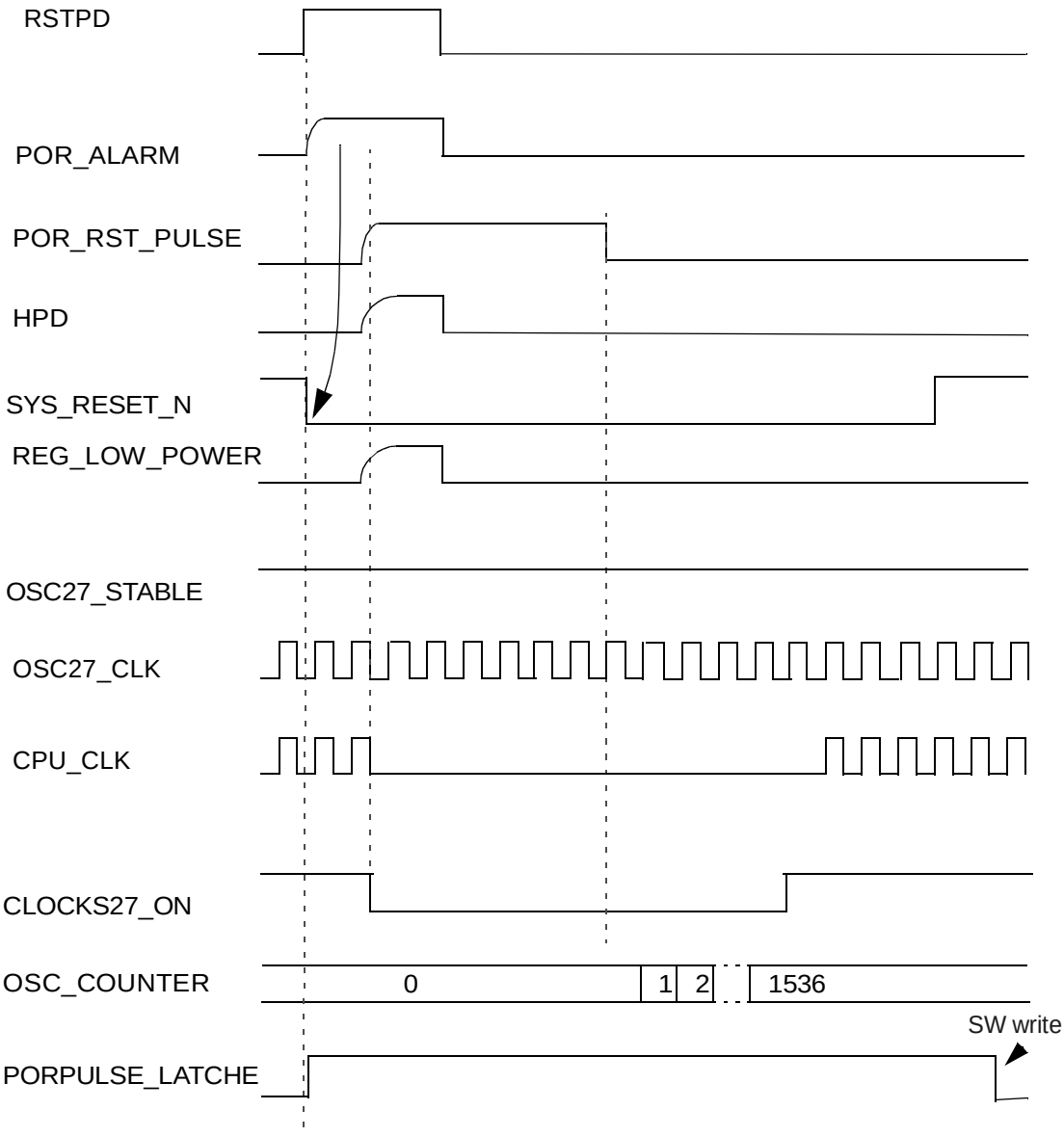


Fig 13. Shut down mode

9.4.7 Power down sequence

Two mode have to be considered: USB or non USB application.

In a USB application, see Figure 14 “Power-down sequence in a USB application” on page 23, embedded firmware shall first stop 96 MHz clocks, then stop the PLL and stop the 4 MHz Oscillator. Then it can execute the power-down sequence

In a non USB application, see Figure 15 “Power Down sequence in a non USB application” on page 24, embedded firmware shall directly start the power-down sequence.

System gets into Power-down mode when CPU writes a 1 into the PD bit in the PCON register in the 80c51. CPU_PD is then asserted. The state machine decides to stop all clocks (CLOCKS27_ON = 0). This will only occur when all clocks are naturally all 0. Finally the REG_LOW_POWER signal is asserted to switch the REGULATOR in low power mode.

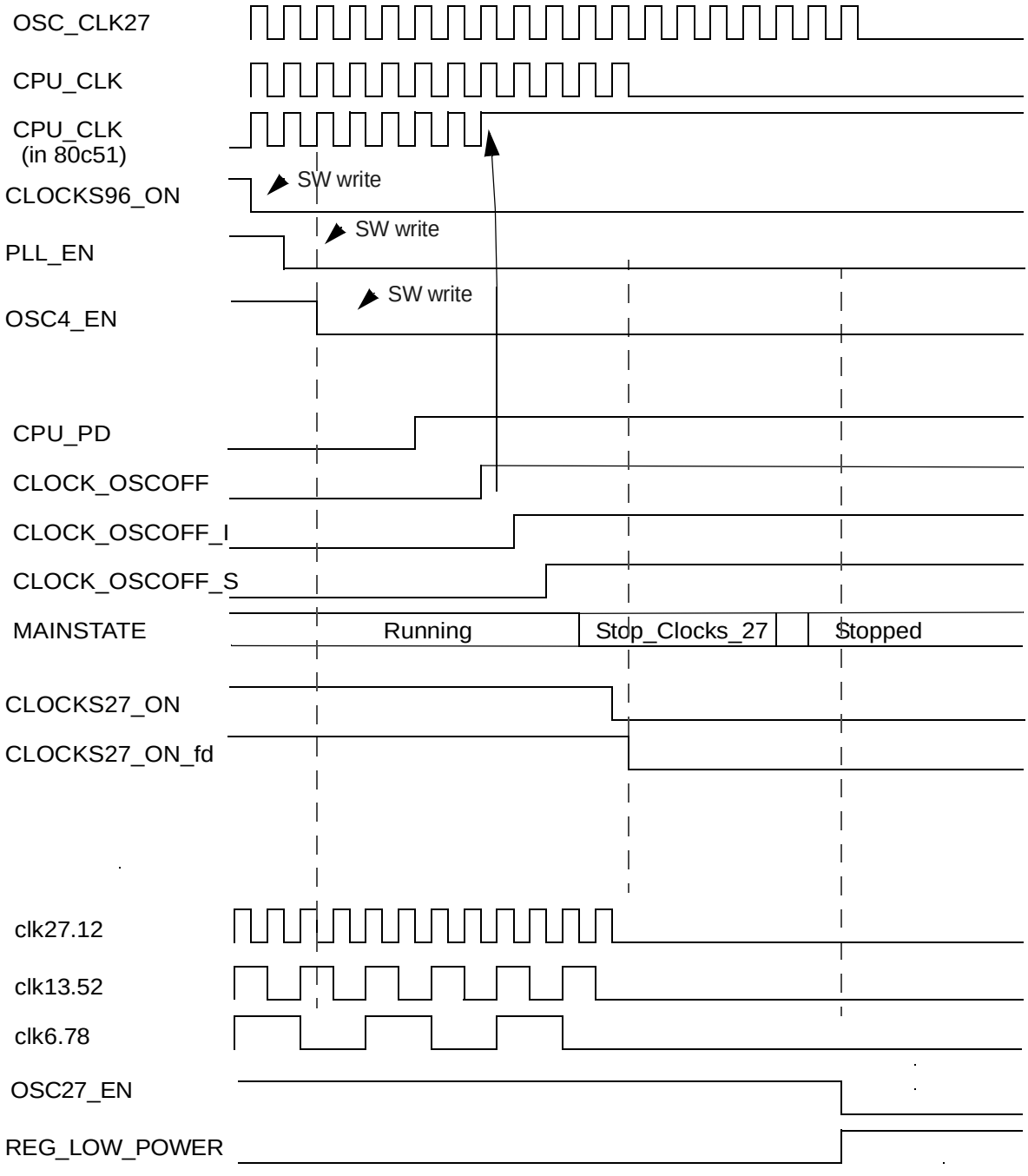


Fig 14. Power-down sequence in a USB application

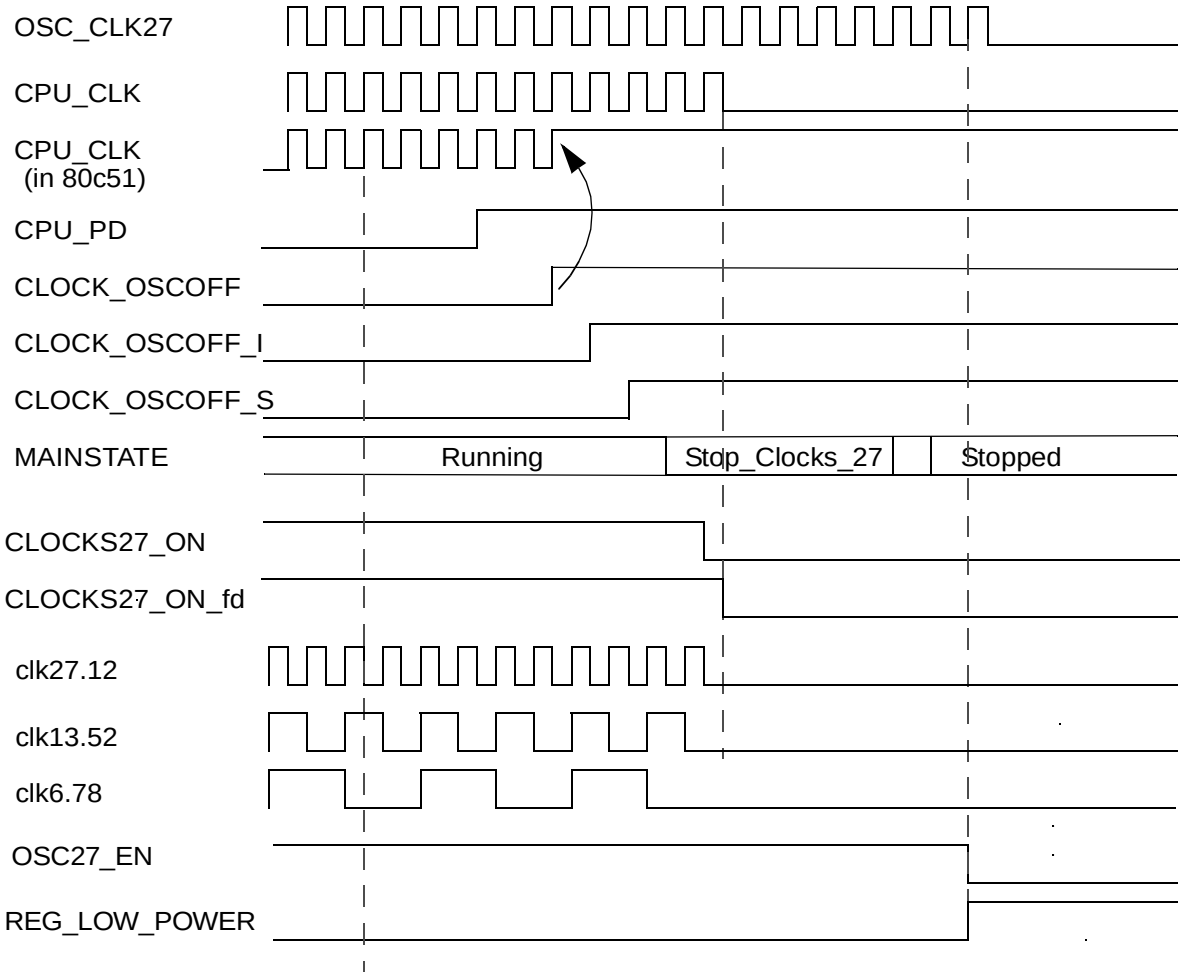


Fig 15. Power Down sequence in a non USB application

9.4.8 Remote wake-up from power-down sequence

System wakes up from Power down mode when one of the wake-up source has been enabled and becomes asserted. There are six wake-up sources (p32_int0, p33_int1, USB clock_on, RF_detect, hsu_on and SPI_on). When one of these signals is asserted and when its corresponding enable bit is set, the internal PCR_wakeup signal is asserted. The wake-up source can be served only if the PCR main state machine is in the Stopped State. If not, the PCR main state machine will wait for that Stopped state before jumping to a Start_OSC27 State to wake-up the system. Once the PCR main state machine has jumped to the Idle state, the state machine waits that the OSC27 is stable (OSC27_STABLE = 1) and then counts1536 edges of OSC_CLK27.

Then it depends on USB or non USB application.

In a non USB application, system is ready to operate (see Figure 16 “Remote wake-up from power-down in a non USB application” on page 25).

In a USB application, see Figure 14 “Power-down sequence in a USB application” on page 23, embedded firmware shall start the 4 MHz oscillator. After a timing controlled by embedded firmware (T5 in USB application diagram) the oscillator has started correctly, embedded firmware shall start the PLL. embedded firmware shall poll the PLL_lock signal to enable the 96 MHz clocks. This defines the T6 timing in the USB application diagram. When the 96 MHz clock is enabled, the 48 MHz clock exists, embedded firmware shall also enable USB clock by setting usb_en to 1. (embedded firmware can also let usb_en = 1 in power-down + remote wake-up)

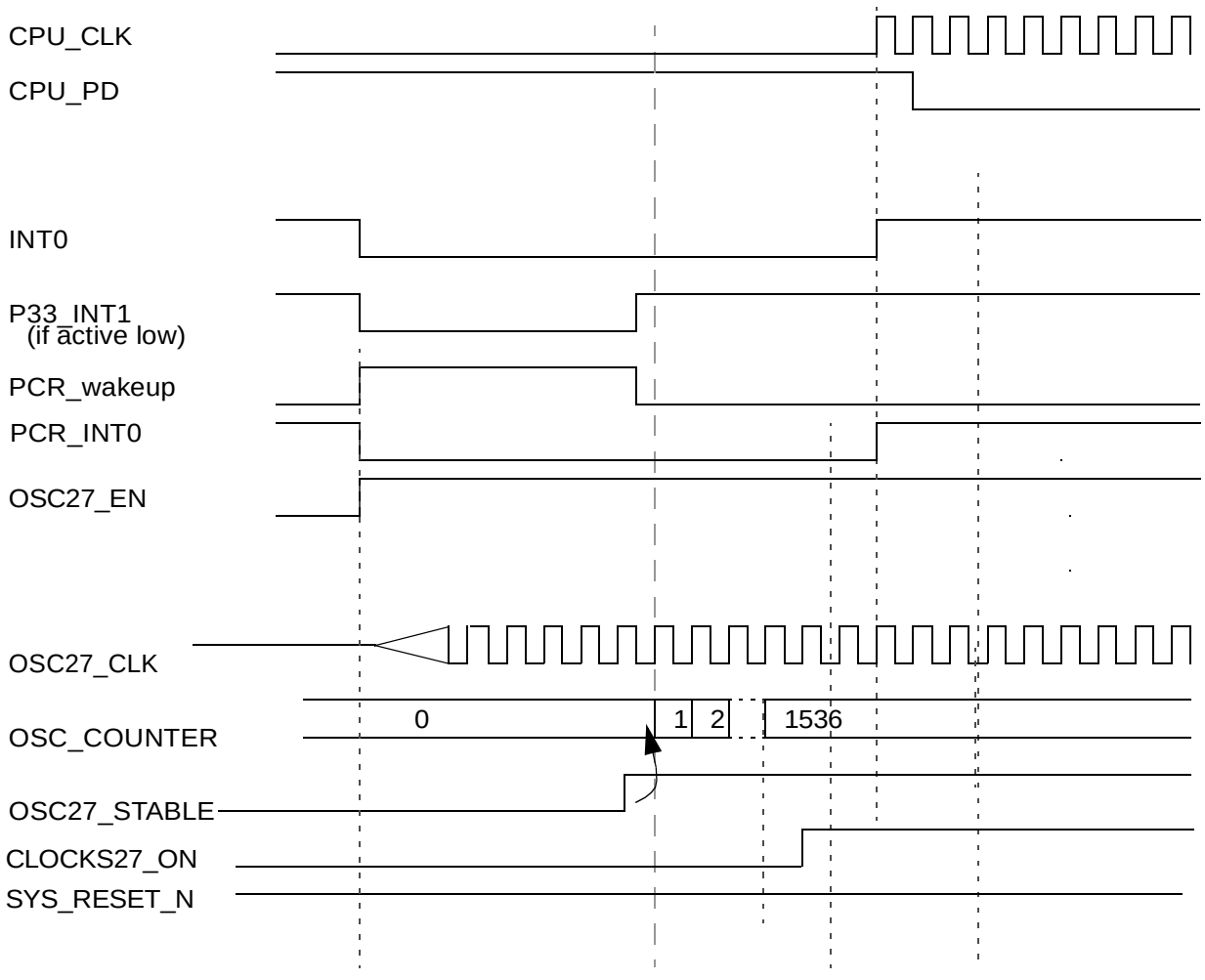


Fig 16. Remote wake-up from power-down in a non USB application

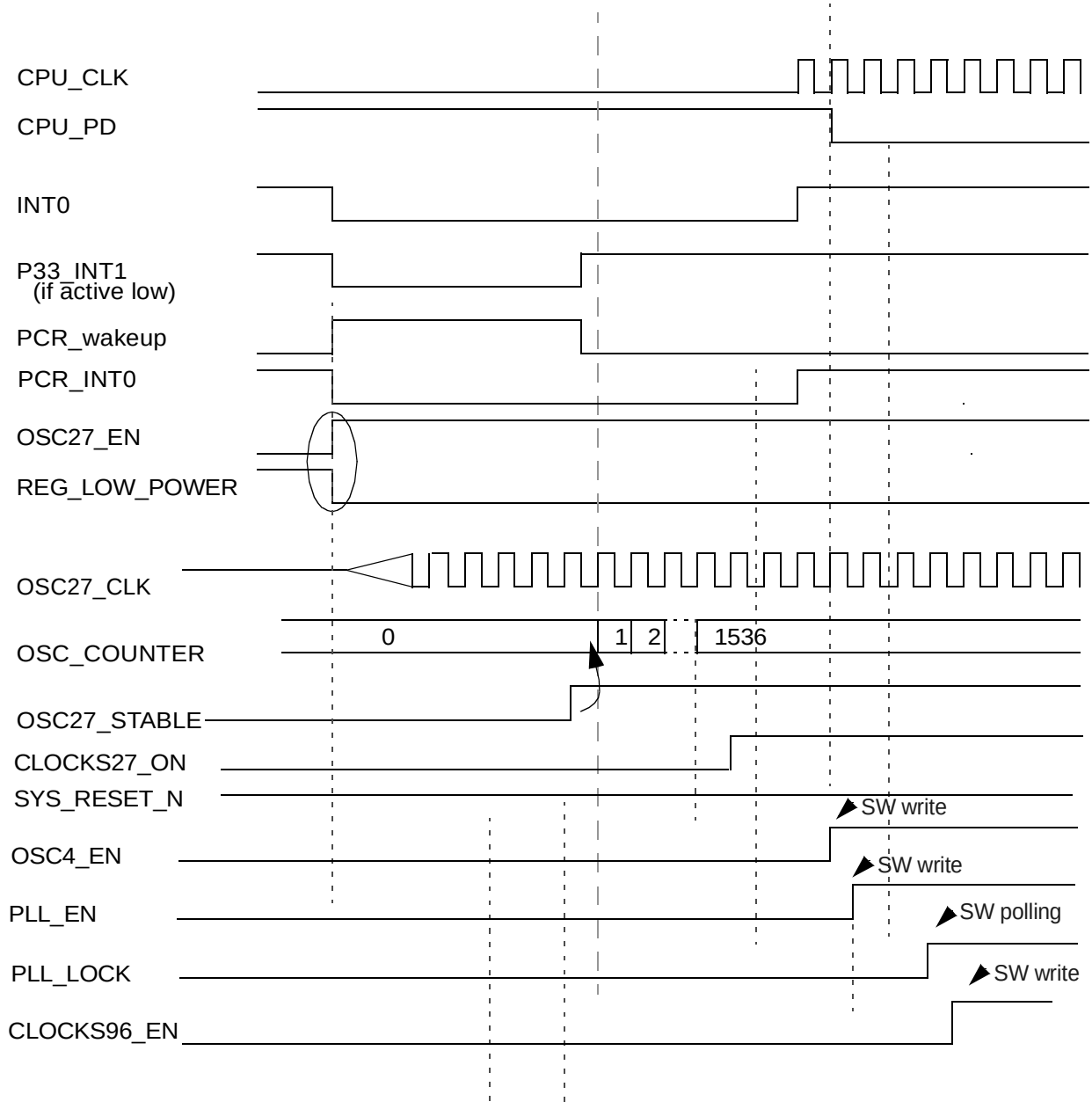


Fig 17. Remote wake-up from power-down in a USB application

9.4.9 PCR Extension Register List

The table enclosed depicts the available registers.

Table 7: PCR Register List

Name	Size [bytes]	Address Offset	Description	Reset	R/W
CFR	1	6200h	Clock Frequency Register	02	R/W
CER	1	6201h	Clock Enable Register	0E	R/W
ILR	1	6202h	Interrupt Level Register	00	R/W
Control	1	6203h	Control	C0	R/W
Status	1	6204h	Status	00	R
Wakeupen	1	6205h	Wake-up Enable	80	R/W

9.4.10 PCR Register Description

9.4.10.1 Register CFR

The Clock Frequency Register is used to select the frequency of the CPU. A default frequency is selected after reset for every block. embedded firmware can write in this register at any time. Hardware support dynamic clock changing.

Table 8: PCR Clock Frequency Register (address 6200h)

Bit	Name	Description	Reset	R/W
7 to 4	-	Reserved		R/W
3 to 2	-	Reserved	00	R/W
1to 0	cpu_frq[1:0]	Select CPU clock frequency	10	R/W

Table 9: cpu_frq[1:0]

cpu_frq[1:0]	CPU clock frequency
00	27.12MHz
01	13.56 MHz
10	6.78 MHz
11	27.12 MHz

9.4.10.2 Register CER

The Clock Enable Register is used to enable or disable the clock of the USB and HSU. By default after reset, all clocks are enabled except the USB one. embedded firmware can write in this register at any time. Hardware supports dynamic clock switching. This register also contains the PLL_lock signal that the embedded firmware will poll.

Table 10: PCR Clock Enable Register (address 6201h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	clock_on	PLL_lock	hsu_enable	-	-	usb_enable
Reset			1	0	1	1	1	0
Access	R/W	R/W	R	R	R/W	R/W	R/W	R/W

Table 11: Description of PCR Clock Enable Register bits

Bit	Symbol	Description
7 to 6	-	Reserved
5	clock_on	**USB clock_on signal to poll** before entering PN531 into power-down. In USB application, when the USB module detect a suspend state (a USB interrupt is generated), this bit has to be polled at 0 before entering PN531 into Power-down mode (stopping all the clocks).
4	PLL_lock	**PLL lock signal.** When 1 PLL is locked. When 0 PLL is unlocked. embedded firmware will poll this bit before enabling the 96 MHz clocks.
3	hsu_enable	**Enable HSU clock.** When 1 HSU is enabled. When 0 HSU is disabled.
2 to 1	-	Reserved
0	usb_enable	**Enable USB clock.** When 1 USB is enabled. When 0 USB is disabled.

9.4.10.3 Register ILR

The Interrupt Level Register is used to program the level of the external interrupts. A default low level interrupt is selected after reset. embedded firmware can write in this register at any time.

Table 12: PCR Interrupt Level Register (address 6202h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	porpulse_latche	-	enable_pdselif	-	gpirq_level	int1_level	int0_level
Reset	1	0	0	0	0	0	0	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 13: Description of PCR Interrupt Level Register bits

Bit	Symbol	Description
7	-	Reserved
6	porpulse_latche	**Indication that a reset has been generated.** When 1, indicates that the system has been reset. Embedded firmware can write a 0 during the embedded firmware reset sequence.
5	-	Reserved
4	enable_pdselif	**Enables MATX host interface power-down control by P33_INT1.** When 1, the state of the pad P33_INT1 controls directly the HZ state of the selected interface of the MATX. If P33_INT1 is at 1, then the output of the selected interface of the MATX are driven according to the protocol of the interface. If P33_INT1 is at 0 then the output of the selected interface of the MATX are set into HZ state.When 0 the pad P33_INT1 does not control the HZ state of the selected interface of the MATX.
3	-	Reserved

Table 13: Description of PCR Interrupt Level Register bits *…continued*

Bit	Symbol	Description
2	gpirq_level	**Select gpirq level interrupt.** When 1, the wake-up condition is true when the gpirq is high. When 0, the wake-up condition is true when the gpirq is low.
1	int1_level	**Select p33_int1 level interrupt.** When 1, the wake-up condition is true when the p33_int1 is high. When 0, the wake-up condition is true when the p33_int1 is low.
0	int0_level	**Select p32_int0 level interrupt.** When 1, the wake-up condition is true when the p32_int0 is high. When 0, the wake-up condition is true when the p32_int0 is low.

9.4.10.4 Register Control

The Control Register is used to perform a embedded firmware reset, to clear wake-up conditions in the Status register, to do the embedded firmware USB reset sequence, to disable internal or external Contact Power off.

Table 14: PCR Control Register (address 6203h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	reset_USB_n	clocks96_on	pll_en	osc4_en	clear_wakeup_cond	soft_reset
Reset	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 15: Description of PCR Control Register bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5	reset_USB_n	**Enables a USB Reset.** When embedded firmware writes a 1, the reset for the USB block is inactive. When embedded firmware writes a 0, the reset for the USB block is active.
4	clocks96_on	**Enables 96 MHz clock generation.** When embedded firmware writes a 1, the 96 MHz clocks are enabled. When embedded firmware writes a 0, the 4 MHz clocks are disabled.
3	pll_en	**Enables the PLL.** When embedded firmware writes a 1, the pll is enabled. When embedded firmware writes a 0, the pll is disabled.
2	osc4_en	**Enables the 4 MHz oscillator.** When embedded firmware writes a 1, the 4 MHz oscillator is enabled. When embedded firmware writes a 0, the 4 MHz oscillator is disabled.
1	clear_wakeup_cond	**Clear the wakeupcond value in Status register.** When embedded firmware writes a 1, the wake-up conditions stored in the PCR status register are cleared. Hardware automatically clears this bit.
0	soft_reset	**Enables a embedded firmware reset.** When embedded firmware writes a 1, the system goes into a embedded firmware reset mode. Hardware clears this bit automatically after performing the embedded firmware reset sequence.

9.4.10.5 Register Status

The Status Register contains the seven wake-up conditions and the extra bit is the clock_on signal that embedded firmware needs to poll before setting a Power-down mode.

Table 16: PCR Status Register (address 6204h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	gpirq_ wake_up	SPI_ wake_up	HSU_ wake_up	CL wake_up	USB_ wake_up	int1_ wake_up	int0_ wake_up
Reset		0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 17: Description of PCR Status Register bits

Bit	Symbol	Description
7	-	Reserved
6	gpirq_ wake_up	**gpirq wake-up source (or function of P34, P35, P50 and P71 signals when respectively enabled and level controlled)**. When 1, indicates that the system woke up from a GÏRQ event (GPIRQ at 0). When 0, indicates that the system woke up from a non GPIRQ event. embedded firmware shall clear this bit after reading it (by writing a 1 to clear_wakeup_cond in PCR control register).
5	SPI_wake_up	**SPI wake-up source (spi_on signal).** When 1, indicates that the system woke-up from a SPI event (NSS at 0). When 0, indicates that the system woke-up from a non SPI event. embedded firmware shall clear this bit after reading it (by writing a 1 to clear_wakeup_cond in PCR control register).
4	HSU_wake_up	**HSU wake-up source (hsu_on signal).** When 1, indicates that the system woke up from a HSU event (5 rising edge on RX). When 0, indicates that the system woke up from a non HSU wake-up event. embedded firmware shall clear this bit after reading it (by writing a 1 to clear_wakeup_cond in PCR control register).
3	CL wake_up	**Contact Less wake-up source (RF_detect signal).** When 1, indicates that the system woke-up from a Contact Less interrupt. When 0, indicates that the system woke-up from a non Contact Less interrupt. embedded firmware shall clear this bit after reading it (by writing a 1 to clear_wakeup_cond in PCR control register).
2	USB_wake_up	**USB wake-up source (clock_on signal).** When 1, indicates that the system woke up from an USB interrupt. When 0, indicates that the system woke up from a non USB interrupt. embedded firmware shall clear this bit after reading it (by writing a 1 to clear_wakeup_cond in PCR control register).
1	int1_wake_up	**p33_int1 wake-up source.** When 1, indicates that the system woke up from a p33_int1 interrupt. When 0, indicates that the system woke up from a non p33_int1 interrupt. embedded firmware shall clear this bit after reading it (by writing a 1 to clear_wakeup_cond in PCR control register).
0	int0_wake_up	**p32_int0 wake-up source.** When 1, indicates that the system woke up from a p32_int0 interrupt. When 0, indicates that the system woke up from a non p32_int0 interrupt. embedded firmware shall clear this bit after reading it (by writing a 1 to clear_wakeup_cond in PCR control register).

9.4.10.6 Register Wakeupen

The Wakeupen Register contains the seven wakeup condition enables.

Table 18: PCR Wakeupen Register (address 6205h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	GPIRQ_wu_en	SPI_on_en	HSU_on_en	rf_detect_en	clock_on_en	int1_en	int0_en
Reset		0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 19: Description of PCR Wakeupen Register bits

Bit	Symbol	Description
7	-	Reserved
6	GPIRQ_wu_en	**General Purpose IRQ wake-up source enable.** When 1, GPIRQ wake-up source can wake-up the system. When 0, GPIRQ wake-up source can not wake-up the system.
5	SPI_on_en	**SPI wake-up source enable.** When 1, SPI_on wake-up source can wake-up the system. When 0, SPI_on wake-up source can not wake-up the system.
4	HSU_on_en	**HSU wake-up source enable.** When 1, hsu_on wake-up source can wake-up the system. When 0, hsu_on wake-up source can not wake-up the system.
3	rf_detect_en	**Contact Less wake-up source enable.** When 1, rf_detect wake-up source can wake-up the system. When 0, rf_detect wake-up source can not wake-up the system.
2	clock_on_en	**USB wake-up source enable.** When 1, clock_on wake-up source can wake-up the system. When 0, clock_on wake-up source can not wake-up the system.
1	int1_en	**p33_int1 wake-up source enable.** When 1, p33_int1 wake-up source can wake-up the system. When 0, p33_int1 wake-up source can not wake-up the system.
0	int0_en	**p32_int0 wake-up source enable.** When 1, p32_int0 wake-up source can wake-up the system. When 0, p32_int0 wake-up source can not wake-up the system.

9.5 80C51

The 80C51 is the microcontroller of PN531. It manages the complete system through several communication links. Several embedded function are implemented in this microcontroller.

9.5.1 Feature list

The main characteristics of the 80C51 are listed here after.

- A Central Processing Unit
- A ROM interface supporting ROM memory.
- A RAM interface supporting specifically Embedded MAIN and XRAM memories.
- A HOST interface for embedded peripherals.
- A Power CONtrol Function module to manage the CPU power consumption.
- A Clock module controlling the CPU clock during Shutdown/Idle and Wake-up mode.
- A PORT module to interface the Control Processing Unit and the IO pads depending of the functional mode (IOs).
- An Interrupt controller.
- Timers 0, 1 and 2.
- An Universal Asynchronous Receiver and Transmitter (Full duplex serial port UART).
- A Master SLave I^2C bus (400 kHz SCL clock).

9.5.2 PN531 Memory Map

The memory map of PN531 is composed of 2 main memory areas. The Data memory area and the Program memory area. The figure enclosed here after depicts the 2 areas and briefly explains the link in between.

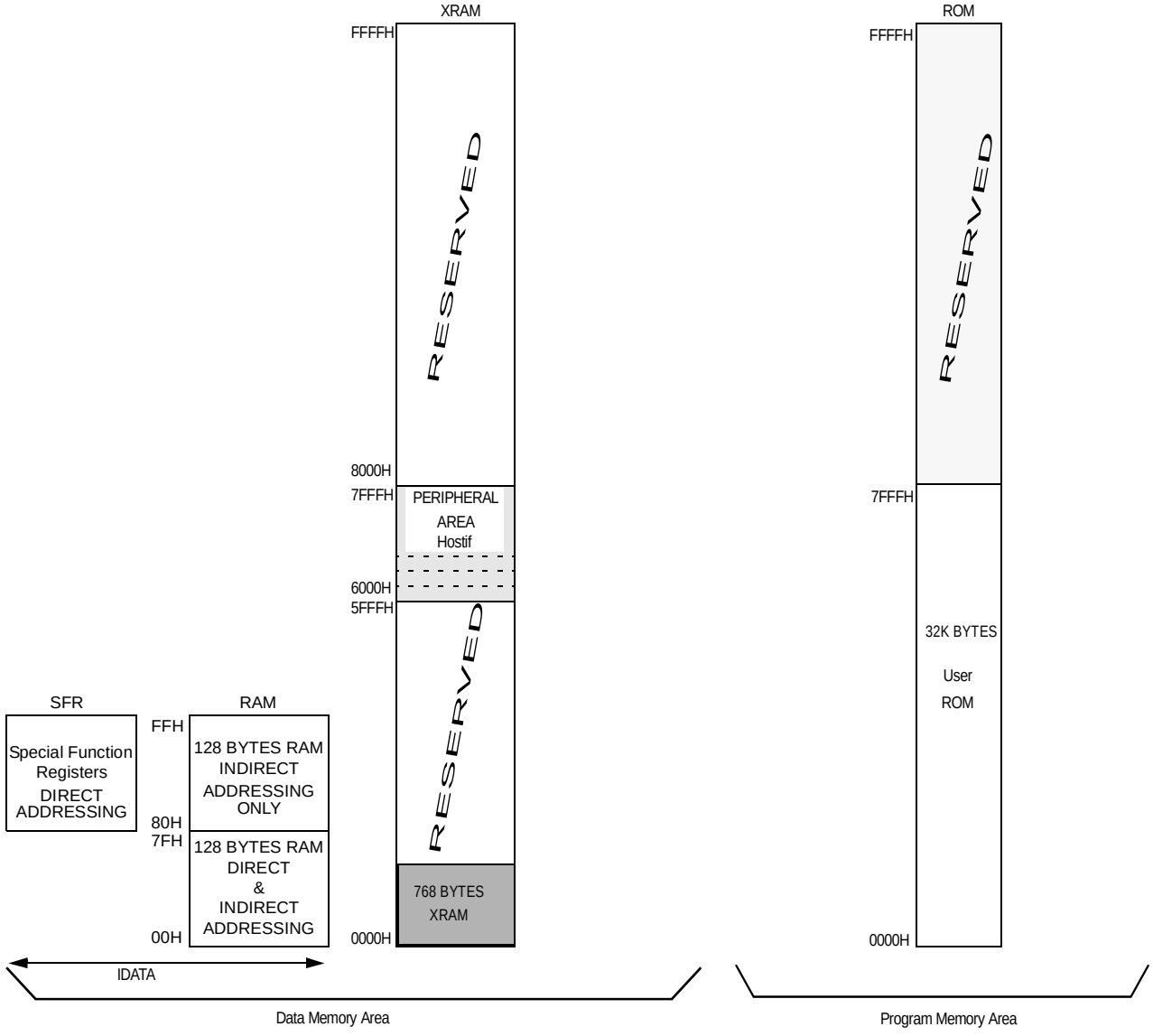


Fig 18. PN531 Memory Map Overview

9.5.2.1 Data Memory

The DATA memory area is divided into 2 areas:

- 256 bytes IDATA memory with one byte wide addresses
- 1 bank of 64 kB extended RAM with two bytes wide addresses for the bank

9.5.2.2 IDATA memory

.The IDATA memory is mapped into three blocks, which are generally referred to as lower 128 bytes, the upper 128 bytes, and the SFRs. These IDATA Memory addresses are always on byte wide, which implies an address space of only 256 bytes. However, the addressing modes for IDATA Memory can in fact accommodate 384 bytes. Direct access higher than 7Fh access one memory space, and indirect addresses higher than 7Fh access a different memory space.Thus the upper 128 and SFR spaces occupy the same block of addresses, 80h through FFh, although they are physically separate entities.
All the bytes in the lower 128 can be accessed by either direct or indirect addressing

Table 20: SFR Map of NFC controller

	↓ **bit-addressable**								
0F8	IP1		XRAMP	**<tbd>**	P3CFGA	P3CFGB	**<tbd>**	**<tbd>**	0FF
0F0	B				P7CFGA	P7CFGB		P7	0F7
0E8	IE1	Status2	FIFOData	FIFOLevel	WaterLevel	Control	BitFraming	Coll	0EF
0E0	ACC				**<tbd>**	**<tbd>**	**<tbd>**		0E7
0D8	I^2C0C0N	I^2C0STA	I^2C0DAT	I^2C0ADR				Status1	0DF
0D0	PSW	Command	commIEn	DIVIEn	CommIrq	DivIrq	Error	P5	0D7
0C8	T2CON	T2MOD	RCAP2L	RCAP2H	T2L	T2H	**<tbd>**	**<tbd>**	0CF
0C0	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	0C7
0B8	IP0	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	0BF
0B0	P3	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	**<tbd>**	0B7
0A8	IE0	SPI_CTR	SPI_ST	HSU_STA	HSU_CTR	HSU_PRE	HSU_CNT	**<tbd>**	0AF
0A0	**<tbd>**	FITEN	FDATA	FSIZE	**<tbd>**	**<tbd>**			0A7
098	S0CON	SBUF	RWL	TWL	FIFOFS	FIFOFF	SFF	FIT	09F
090	**<tbd>**				**<tbd>**	**<tbd>**			097
088	T01CON	T01MOD	T0L	T1L	T0H	T1H			08F
080	**<tbd>**	SP	DPL	DPH	**<tbd>**	**<tbd>**		PCON	087

Remark: NFC controller specific SFRs

9.5.2.3 XRAM memory

The XRAM memory space is divided into 2 memory spaces reserved for accessing different modules having different characteristics.

The XRAM memory area is divided into 2 areas as follow:

- The XRAM memory space from 0000h to 5FFFh is reserved to address the embedded RAM. PN531 implements only a 768 bytes memory in that area (from 0000h to 02FFh).
- The XRAM memory space from 6000h to 7FFFh is reserved to address the embedded peripherals. This address space is divided into 32 regions of 256 bytes each. Very simple addressing can be performed using R0 or R1 and the XRAM SFR. This area is reserved for internal peripherals.

The Table 21 “Peripheral mapping into XRAM memory space” on page 35 despicts the internal peripheral memory mapping into the XRAM memory space.

Table 21: Peripheral mapping into XRAM memory space

Base Address	End address	Description
6000h	60FFh	Internal USB peripheral Refer to Section 9.13 “USB” on page 100
6100h	61FFh	IOs and miscellaneous registers configuration Refer to Section 9.9 “IOs configuration and Miscellaneous registers” on page 61
6200h	62FFh	Power Clock and Reset controller Refer to Section 9.4.9 “PCR Extension Register List” on page 27
6300h	7FFFh	Reserved
8000h	FFFFh	Reserved

The XRAM memory space is accessible by the dedicated MOVX instructions. According to the 80C51 standard these instructions feature the active working registers R0 and R1 as address pointers for the lower 256 XRAM bytes (0 to FFh). The full XRAM address space is accessible via the data pointer DPTR.

PN531 features a banking mechanism for the XRAM access with R0 and R1. Thanks to the SFR XRAMP providing the upper byte of the address given by R1 or R0.

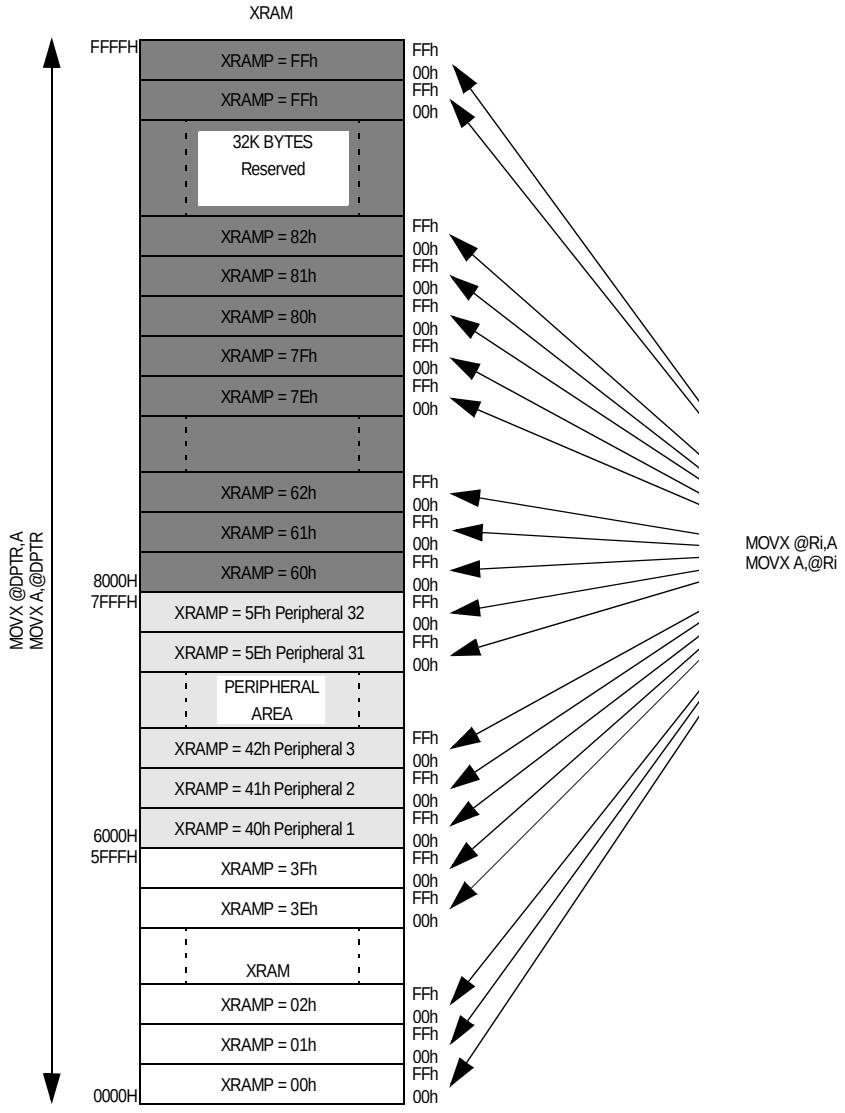


Fig 19. Indirect Addressing of XRAM memory space

9.5.2.4 EXRAM memory

PN531 does not support this memory space.

9.5.2.5 Program Memory

The program memory space for PN531 is in a range from 0000h to 7FFFh. Within this range ROM memory is selected.

9.5.3 Central Processing Unit

The Central Processing Unit include the following blocks:

- A State counter
- A Control Unit
- An Arithmetic Logic Unit
- A Program Counter
- An Instruction Register
- An SFR address Register
- An SFR bit Register
- An Stack Pointer Register

9.5.3.1 State Counter

The State counter (STC) generates the states and cycles for the CPU timing. It consists of a sleep state counter (which is active during idle mode), and a normal state and cycle counter (which are stopped during the idle mode).

9.5.3.2 Control Unit

Each instruction is divided into a number of microinstructions. To create an instruction, the control Unit (UCTRL) outputs the appropriate sequence of control signals to send data through the logic blocks of the CPU at the proper time. The control unit is driven by the contents of the instruction register and by the state and cycle counters.

9.5.3.3 Arithmetic Logic Unit

The ALU performs the arithmetic operations.

9.5.3.4 Program Counter

The PC generates the next program memory address.

9.5.3.5 Instruction Register

The IR holds the opcode of the instruction in progress.

9.5.3.6 SFR Address Register

The SAR holds the address of the Special Function Register that is selected for the next read or write operation.

9.5.3.7 SFR Bit Register

The SBR holds the number of the bit that is selected for the next bit operation on a SFR. This value is used by the ALU to select the proper bit mask.

9.5.3.8 Stack Pointer

The SP holds the stack pointer.

9.5.3.9 Instruction map

The Table 22 “SmartMX 80C51 Instruction map” on page 38 depicts the hexadecimal opcode cross-reference.

Table 22: Smart*MX* 80C51 Instruction map

First hexadecimal chaRacter of opcode	← Second hexadecimal chaRacter of opcode →															
↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	INC @Ri 1	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	DEC @Ri 1	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	ADD A,@Ri 1	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
3	JBC bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	ADDC A,@Ri 1	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	ORL A,@Ri 1	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	JNC rel	ACALL addr11	ANL direct	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	ANL A,@Ri 1	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	XRL A,@Ri 1	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	MOV @Ri,#data 1	MOV Rr,#data 0	MOV Rr,#data 1	MOV Rr,#data 2	MOV Rr,#data 3	MOV Rr,#data 4	MOV Rr,#data 5	MOV Rr,#data 6	MOV Rr,#data 7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	MOV direct,@Ri 1	MOV direct,Rr 0	MOV direct,Rr 1	MOV direct,Rr 2	MOV direct,Rr 3	MOV direct,Rr 4	MOV direct,Rr 5	MOV direct,Rr 6	MOV direct,Rr 7
9	MOV DPTR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	SUBB A,@Ri 1	SUB A,Rr 0	SUB A,Rr 1	SUB A,Rr 2	SUB A,Rr 3	SUB A,Rr 4	SUB A,Rr 5	SUB A,Rr 6	SUB A,Rr 7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB	reserved	MOV @Ri,direct 0	MOV @Ri,direct 1	MOV Rr,direct 0	MOV Rr,direct 1	MOV Rr,direct 2	MOV Rr,direct 3	MOV Rr,direct 4	MOV Rr,direct 5	MOV Rr,direct 6	MOV Rr,direct 7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	CJNE @Ri,#data,rel 1	CJNE Rr,#data,rel 0	CJNE Rr,#data,rel 1	CJNE Rr,#data,rel 2	CJNE Rr,#data,rel 3	CJNE Rr,#data,rel 4	CJNE Rr,#data,rel 5	CJNE Rr,#data,rel 6	CJNE Rr,#data,rel 7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	XCH A,@Ri 1	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	XCHD A,@Ri 1	DJNZ Rr,rel 0	DJNZ Rr,rel 1	DJNZ Rr,rel 2	DJNZ Rr,rel 3	DJNZ Rr,rel 4	DJNZ Rr,rel 5	DJNZ Rr,rel 6	DJNZ Rr,rel 7
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri 0	MOVX A,@Ri 1	CLR A	MOV A,direct	MOV A,@Ri 0	MOV A,@Ri 1	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A 0	MOVX @Ri,A 1	CPL A	MOV direct,A	MOV @Ri,A 0	MOV @Ri,A 1	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7

9.5.4 ROM Interface

The user ROM memory space is limited to 32 kB.

9.5.5 XRAM Interface

A single SRAM instance is directly attached to the RAM interface module.

The RAM Interface supports a division of the total RAM capacity into:

- MAIN-RAM: 256 bytes of fast accessible internal data memory
- AUX-RAM: a 728 bytes of internal data memory

The RAM Interface supports a page mechanism for AUXRAM access with MOV @R0/1 instructions. The address supplied by R0/1 is extended by the contents of a Ram page Special Function Register (XRAMP).

9.5.6 PCON module

The Power control (PCON) module uses one SFR that control various part of the 80C51. All bits can be read and written by the CPU.

- Setting the 80c51 into IDLE mode.
- Setting the 80c51 into POWER DOWN mode.

Table 23: PPCON Register (address xxxxh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SMOD						PD	IDL
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 24: Description of PCON Register bits

Bit	Symbol	Description
7	SMOD	**Serial MODe:** When this bit is set, it doubles the baud rate of the UART
6 to 3	0	Reserved.
1	PD	**Power-down:** When this bit becomes set, the microcontroller goes in POWER DOWN mode
0	IDL	**Idle:** When this bit becomes set, the microcontroller goes in IDLE mode

9.6 Interrupt Controller

The interrupt controller implemented is targeted to support a large range of application.

9.6.1 Feature list

The interrupt controller has the following functionality:

- 15 interrupt sources are available.
- Incrementing interrupt vector polling scheme.
- Interrupt Enable registers IE0 and IE1.
- Interrupt Priority registers IP0 and IP1.

- Interrupt request line sampling, polling, prioritizing and checking for interrupt blocking conditions.
- Output of a forced LCALL {interrupt vector} instruction to the processor data bus, signal interrupt service to CPU.
- Generation of interrupt acknowledge signals to clear timer01 interrupt request flags on interrupt service.
- Signal interrupt status to timer01 to enable wake-up from POWERDOWN state.
- Signal interrupt service to PCON to terminate IDLE state.

9.6.2 Interrupt vectors

The interrupt vectors are linked to the interrupt sources. The table here after depicts the relationship.

Table 25: Interrupt vector

Interrupt number	Interrupt Vector	Interrupt sources	Priority Level (incremental)
0	0003h	External INT0 (p32_int0 pin) and CPU wake-up during power-down	Highest
1	000Bh	Timer 0 interrupt	
2	0013h	External INT1 (p33_int1 pin)	
3	001Bh	Timer 1 interrupt	
4	0023h	UART interrupt	
5	002Bh	Timer 2 interrupt	
6	0033h	Reserved	
7	003Bh	Reserved	
8	0043h	Reserved	
9	004Bh	CL interrupt 1	
10	0053h	CL interrupt 0	
11	005Bh	I^2C interrupt	
12	0063h	SPI interrupt, FIFO interrupt, HSU interrupt	
13	006Bh	USB interrupt	
14	0073h	General Purpose IRQ (or function of P34, P35, NSS (P50) and MISO(P71) after there respective enable and level control bits)	Lowest

9.6.3 Interrupt Enable

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in IE0 or IE1. A global interrupt enable bit can be cleared to disable all interrupts at once.

9.6.4 Interrupt priority

Each interrupt source can be individually programmed to one of the two priority levels by setting or clearing a bit in IP0 or IP1.

9.6.5 Interrupt Prioritisation

An interrupt can be interrupted by a higher level priority interrupt, but not by an interrupt with an equal or lower level priority. A highest priority level interrupt cannot be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt requests of the same priority level are received simultaneously, a fixed incremental prioritization scheme determines which request is serviced. Refer to Table 25 “Interrupt vector” on page 40 for details.

A RETI (Return From Interrupt) instruction causes the program to continue at the address of the instruction immediately after the point at which the interrupt was detected. If a lower or same level interrupt has been pending when the RETI instruction is executed, then one further instruction of the interrupted program will be executed before the pending interrupt is processed. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in IE0 or IE1. This register also contains a global interrupt enable bit which can be cleared to disable all interrupts at once.

The interrupt controller is control through few SFRs registers.

9.6.6 Register IE0

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in IE0. This register also contains a global interrupt enable bit which can be cleared to disable all interrupts at once.

Table 26: Interrupt controller IE0 Register (address xxxxh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IE0_7	IE0_6	IE0_5	IE0_4	IE0_3	IE0_2	IE0_1	IE0_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 27: Description of Interrupt controller IE0 Register bits

Bit	Symbol	Description
7	IE0_7	When set to 1, makes a global Interrupt enable
6	IE0_6	When set to 1, enables interrupt number 6
5	IE0_5	When set to 1, enables interrupt number 5
4	IE0_4	When set to 1, enables interrupt number 4
3	IE0_3	When set to 1, enables interrupt number 3
2	IE0_2	When set to 1, enables interrupt number 2
1	IE0_1	When set to 1, enables interrupt number 1
0	IE0_0	When set to 1, enables interrupt number 0

9.6.7 Register IE1

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in IE1.

Table 28: Interrupt controller IE1 Register (address xxxxh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IE1_7	IE1_6	IE1_5	IE1_4	IE1_3	IE1_2	IE1_1	IE1_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 29: Description of Interrupt controller IE1 Register bits

Bit	Symbol	Description
7	IE1_7	When set to 1, enables interrupt number 14
6	IE1_6	When set to 1, enables interrupt number 13
5	IE1_5	When set to 1, enables interrupt number 12
4	IE1_4	When set to 1, enables interrupt number 11
3	IE1_3	When set to 1, enables interrupt number 10
2	IE1_2	When set to 1, enables interrupt number 9
1	IE1_1	When set to 1, enables interrupt number 8
0	IE1_0	When set to 1, enables interrupt number 7

9.6.8 Register IP0

Each interrupt source can be individually programmed to one of two priority levels by programming a bit in the Interrupt priority SFRs.

Table 30: Interrupt controller IP1 Register (address xxxxh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IP0_7	IP0_6	IP0_5	IP0_4	IP0_3	IP0_2	IP0_1	IP0_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 31: Description of Interrupt controller IP1 Register bits

Bit	Symbol	Description
7	IP0_7	Reserved.
6	IP0_6	When set to 1, interrupt number 6 gets high priority level. When set to 0, interrupt number 6 gets low priority level.
5	IP0_5	When set to 1, interrupt number 5 gets high priority level. When set to 0, interrupt number 5 gets low priority level.
4	IP0_4	When set to 1, interrupt number 4 gets high priority level. When set to 0, interrupt number 4gets low priority level.
3	IP0_3	When set to 1, interrupt number 3 gets high priority level. When set to 0, interrupt number 3 gets low priority level.
2	IP0_2	When set to 1, interrupt number 2 gets high priority level. When set to 0, interrupt number 2 gets low priority level.
1	IP0_1	When set to 1, interrupt number 1 gets high priority level. When set to 0, interrupt number 1 gets low priority level.
0	IP0_0	When set to 1, interrupt number 0 gets high priority level. When set to 0, interrupt number 0 gets low priority level.

9.6.9 Register IP1

Each interrupt source can be individually programmed to one of two priority levels by programming a bit in the Interrupt priority SFRs.

Table 32: Interrupt controller IP1 Register (address xxxxh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IP1_7	IP1_6	IP1_5	IP1_4	IP1_3	IP1_2	IP1_1	IP1_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 33: Description of Interrupt controller IP1 Register bits

Bit	Symbol	Description
7	IP1_7	When set to 1, interrupt number 14 gets high priority level. When set to 0, interrupt number 14 gets low priority level.
6	IP1_6	When set to 1, interrupt number 13 gets high priority level. When set to 0, interrupt number 13 gets low priority level.
5	IP1_5	When set to 1, interrupt number 12 gets high priority level. When set to 0, interrupt number 12 gets low priority level.
4	IP1_4	When set to 1, interrupt number 11 gets high priority level. When set to 0, interrupt number 11 gets low priority level.
3	IP1_3	When set to 1, interrupt number 10 gets high priority level. When set to 0, interrupt number 10 gets low priority level.
2	IP1_2	When set to 1, interrupt number 9 gets high priority level. When set to 0, interrupt number 9 gets low priority level.
1	IP1_1	When set to 1, interrupt number 8 gets high priority level. When set to 0, interrupt number 8 gets low priority level.
0	IP1_0	When set to 1, interrupt number 7 gets high priority level. When set to 0, interrupt number 7 gets low priority level.

9.7 UART

The Universal Asynchronous Receiver and Transmitter is implemented to facilitate link to other peripherals for diagnose using P30 and P31.

9.7.1 Feature list

The characteristics of the UART are the following:.

- Full duplex serial port
- Receive buffered to allow reception of a second byte while the first byte is being unloaded
- Four modes of operation allow 8 bits and 9 bits data transfers at various baud rates
- Supports multiprocessor communication
- Baud rate can be controlled through Timer1 or Timer2 baud rate generator

9.7.2 UART Functional Description

The UART module is an Asynchronous Universal Receiver Transmitter. It is a full duplex serial port which means it can transmit and receive simultaneously. The serial port is receive-buffered: it can start reception of a second byte before a previously received byte has been read from the receive buffer. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

The serial port receive and transmit data registers are both accessed by embedded firmware at the address of Special Function Register S0BUF. Writing to S0BUF loads the transmit register, reading from S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes. These modes are selected by programming special function register S0CON bits SM0 and SM1.

- Mode 0:
  - Serial data enters through input rxin and exits through output uart_rxout (both connected to pin RxD). Output uart_txout (connected to pin TxD) outputs the shift clock. 8 bits are transmitted/received (LSB first)

    Baud rate: fixed at 1/6 of the frequency of the CPU clock
- Mode 1:
  - 10 bits are transmitted through uart_txout or received through rxin: a start bit (0), 8 data bits (LSB first), and a stop bit (1)
  - Receive: The received stop bit is stored into special function register bit S0CON.RB8
  - Baud rate: variable, set by the rate of either inputs trigger1 or trigger2
- Mode 2:
  - 11 bits are transmitted through uart_txout or received through rxin: start bit (0), 8 data bits (LSB first), a 9th data bit, and a stop bit (1)
  - Transmit: the 9th data bit is taken from S0CON.TB8, it can be assigned the value of 0 or 1. For example, the parity bit could be loaded into S0CON.TB8
  - Receive: the 9th data bit is stored into S0CON.RB8, while the stop bit is ignored
  - Baud rate: programmable to either 1/16 or 1/32 the frequency of the CPU clock

- Mode 3:
  - 11 bits are transmitted through uart_txout or received through rxin: a start bit (0), 8 data bits (LSB first), a 9th data bit, and a stop bit (1).In fact, mode 3 is the same as mode 2 in all aspects except the baud rate
  - Transmit: as mode 2, the 9th data bit is taken from S0CON.TB8
  - Receive: as mode 2, the 9th data bit is stored into S0CON.RB8
  - Baud rate: variable, set by the rate of either inputs trigger1 or trigger2

The UART initiates transmission and/or reception as follows.

- Transmission is initiated, in modes 0, 1, 2, 3, by any instruction that uses S0BUF as destination
- Reception is initiated, in mode 0, if S0CON.RI = 0 and S0CON.REN = 1
- Reception is initiated in modes 1, 2, 3 by the incoming start bit if S0CON.REN = 1

The UART contains 2 SFRs:

Table 34: UART SFR Register List

Name	Size [bytes]	SFR Address	Description	Access
S0CON	1	0098h	Control and status register	R/W
S0BUF	1	0099h	Transmit and receive buffer	R/W

9.7.3 Register S0CON

The Special Function Register S0CON is the control and status register of the UART. This register contains the mode selection bits (SM2, SM1, SM0), the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 35: UART S0CON Register (SFR: address 98h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SM (0:1)	SM2	REN	TB8	RB8	TI	TI	SM (0:1)
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 36: Description of UART S0CON Register bits

Bit	Symbol	Description
7	SM (0:1)	**Mode selection bit 0 and 1.** Set/cleared by embedded firmware only. The UART has 4 modes (see Table 37 “UART modes”).
6	SM2	**Multiprocessor communication enable.** Enables the multi processor communication feature in modes 2 and 3. Set/cleared by embedded firmware only.In modes 2 or 3, if SM2 is set, then RI will not be activated and RB8 and S0BUF will not be loaded if the received 9th data bit is 0, if SM2 is cleared it has no influence n the activation of RI and RB8.In mode 1, if SM2 is set, then RI will not be activated and RB8 and S0BUF will not be loaded if no valid stop bit was received, if SM2 is cleared it has no influence on the activation of RI and RB8. In mode 0, SM2 has no influence.
5	REN	**Serial reception enable.** Set/cleared by embedded firmware only. Enables serial reception. Set by embedded firmware enables reception. Cleared by embedded firmware disables reception.

Table 36: Description of UART S0CON Register bits *...continued*

Bit	Symbol	Description
4	TB8	**Transmit data bit.** Set/cleared by embedded firmware only. The value of TB8 is transmitted as the 9th data bit in modes 2 and 3. The TB8 bit is not used in modes 0 and 1. Set or cleared by embedded firmware as desired.
3	RB8	**Receive data bit.** Set/cleared by hardware and by embedded firmware (if SM2=1 loading RB8 can be blocked, see bit description of SM2 above).In modes 2 or 3, the hardware stores the 9th data bit that was received in RB8.In mode 1, the hardware stores the stop bit that was received in RB8.In mode 0, the hardware does not change RB8.
2	TI	**Transmit interrupt flag.** In modes 2 or 3, when transmitting, the hardware sets the transmit interrupt flag TI at the end of the 9th bit time.In modes 0 or 1, when transmitting, the hardware sets the transmit interrupt flag TI at the end of the 8th bit time.TI must be cleared by embedded firmware.
1	RI	**Receive interrupt flag.** In modes 2 or 3, when receiving, the hardware sets the receive interrupt flag 1 clock period after sampling the 9th data bit (if SM2=1 setting RI can be blocked, see bit description of SM2 above). In mode 1, when receiving, the hardware sets the receive interrupt flag 1 clock period after sampling the stop bit (if SM2=1 setting RI can be blocked, see bit description of SM2 above).In mode 0, when receiving, the hardware sets RI at the end of the cpu state 1 of the 9th machine cycle after the machine cycle where the data reception started by a write to S0CONRI must be cleared by embedded firmware.
0	SM (0:1)	**Mode selection bit 0 and 1.** Set/cleared by embedded firmware only. The UART has 4 modes (see Table 37 “UART modes”).

Remark: The S0CON register supports a locking mechanism to prevent embedded firmware read-modify-write instructions to overwrite the contents while hardware is modifying the contents of the register.

Table 37: UART modes

Mode	SM0	SM1	Description	Baud rate
0	0	0	Shift register	fclk/6
1	0	1	8 bits UART	Variable
2	1	0	9 bits UART	fclk/64 or fclk/32
3	1	1	9 bits UART	Variable

9.7.4 Register S0BUF

This register is implemented twice. Writing to S0BUF writes to the transmit buffer. Reading from S0BUF reads from the receive buffer. Only hardware can read from the transmit buffer and write to the receive buffer.

Table 38: UART S0BUF Register (SFR: address 99h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	S0BUF							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 39: Description of UART S0BUF Register bits

Bit	Symbol	Description
7 to 0		**Writing to S0BUF writes to the transmit buffer.** Reading from S0BUF reads from the receive buffer.

9.7.5 Baud Rate

The serial port can operate with different baud rates depending on its mode:

- **Mode 0:**
  the baud rate is derived from cpu_state2 and cpu_state5 and thus fixed:
  - Baud rate = CLK/6

The next table lists the baud rates in UART mode 0.

Table 40: Baud rates in mode 0

Conditions	Min	Typ	Max	Unit
f_{CLK}	6.78	13.56	27.12	MHz
Baud rate	1.13	2.26	4.52	MHz

- **Mode 2:**
  the baud rate is in mode 2 depends on the value of bit SMOD.
  - If SMOD = 0, the baud rate is fclk/$_{32}$
  - If SMOD = 1, the baud rate is fclk/$_{16}$

Baud rate = $\frac{2^{SMOD}}{32} \times f_{clk}$

The next table lists the baud rates in UART mode 2.

Table 41: Baud rates in mode 2

Conditions	Min	Typ	Max	Unit
f_{CLK}	6.78	13.56	27.12	MHz
Baud rate (SMOD=0)	212	423	847	MHz
Baud rate (SMOD=1)	423	847	1.69	MHz

Mode 1 and 3: The baud rates are determined by the rate of the inputs *trigger1* and *trigger2*.The input ttrigger2en selects if trigger1 or trigger2 should be used as a source when transmitting. The input rtrigger2en selects if trigger1 or trigger2 should be used as a source when receiving.

Mode 1, 3 baud rate = 2SMOD/32 * trigger1 rate.

Mode 1, 3 baud rate = 1/16 * trigger2 rate.

The next table shows the trigger select:

Table 42: Trigger select

rtrigger2en	ttrigger2en	SMOD	receive trigger rate	transmit trigger rate
	-	0	trigger1/32	-
	-	1	trigger1/16	-
	-	-	trigger1/16	-
-	0	0	-	trigger1/32
-	0	1	-	trigger1/16
-	1	-	-	trigger2/16

The rates listed in the table above are valid when the pattern on input *trigger1* is a pulse of 1 *CLK* period high. If input trigger is high for more than 2 *CLK* periods and SMOD = 0, the resulting trigger signal gets a pattern of half the *CLK* frequency. The next figure shows how the *trigger1* division is done by the UART (the resulting trigger is *trigger1/2* in the figure).The next figure shows the implementation of the trigger division logic as a state diagram. Note that the output of the state diagram “trigger1/2” is only asserted when the state machine is in state 0 and SMOD is low and *trigger1* is high.

The next figure shows the implementation of the trigger division logic as a state diagram. Note that the output of the state diagram “trigger1/2” is only asserted when the state machine is in state 0 and SMOD is low and trigger1 is high.

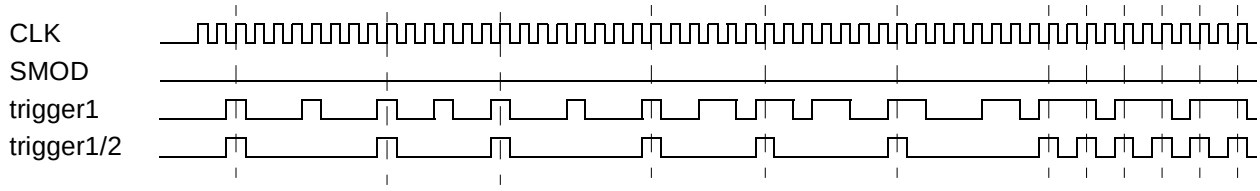


Fig 20. Trigger division waveform

The next figure shows the implementation of the trigger division logic as a state diagram. Note that the output of the state diagram “trigger1/2” is only asserted when the state machine is in state 0 and SMOD is low and trigger1 is high.

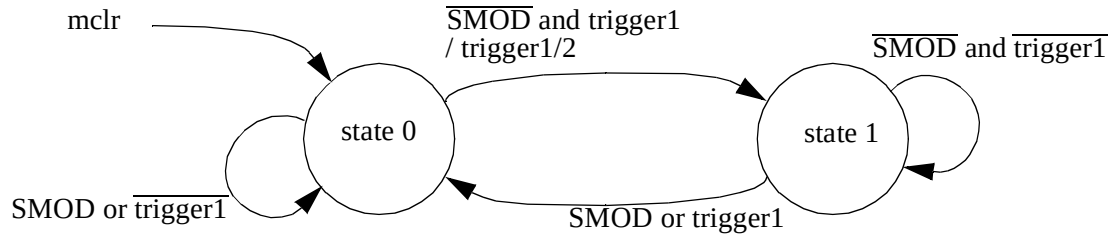


Fig 21. Trigger division state diagram

The next table lists the baud rates in mode 1 and 3 using input trigger1 for two different rates of trigger1 (with a pulse high width of 1 CLK period).

Table 43. Baud rates in mode 1 and 3 using input trigger1

Conditions	Min	Typ	Max	Unit
f_{CLK}	6.78	13.56	27.12	MHz
Baud rate (SMOD=0, $f_{trigger1} = f_{CLK}/6$)	35.3	70.6	141.2	kHz
Baud rate (SMOD=1, $f_{trigger1} = f_{CLK}/6$)	70.6	141.2	282.5	kHz
Baud rate (SMOD=0, $f_{trigger1} = f_{CLK}/12$)	17.65 kHz	35.3 kHz	70.6 MHz	
Baud rate (SMOD=1, $f_{trigger1} = f_{CLK}/12$)	35.3 kHz	70.6 kHz	141.2 MHz	

The next table lists the baud rates in mode 1 and 3 using input trigger2 for two different rates of trigger2 (with a pulse high width of 1 CLK period).

Table 44. Baud rates in mode 1 and 3 using input trigger2

Conditions	Min	Typ	Max	Unit
f_{CLK}	6.78	13.56	27.12	MHz
Baud rate (SMOD=0, $f_{trigger2} = f_{CLK}/12$)	35.3	70.6	141.2	kHz
Baud rate (SMOD=1, $f_{trigger2} = f_{CLK}/6$)	70.6	141.2	282.5	kHz

9.7.5.1 Baud rates using timer 1 (UART mode 1 and 3)

The overflow output 't01_t1ov' of timer 1 of the 80c51 timer01 module can be used to drive the UART input pin trigger1. The UART must be set in mode 1 or 3 and the input ttrigger2en must be 0 to select trigger1 for transmitting and the input rtrigger2en must be 0 to select trigger1 for receiving. The timer 1 interrupt should be disabled in this application. The timer 1 itself can be configured for either 'timer' or 'counter' operation, and in any of its 3 running modes. In the most typical applications, it is configured for 'timer' operation, in the auto-reload mode (timer 1 mode 2: high nibble of T01MOD = 0010b). In that case the baud rate is given by the formula:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{f_{clk}}{6 \times (256 - T1H)}$$

When rewriting this formula, the value for the timer 1 reload value T1H is calculated from the desired baud rate as follows:

$$\text{Timer 1 reload value T1H} = 256 - \frac{2^{SMOD} \times f_{clk}}{32 \times 6 \times Baudrate}$$

One can achieve very low baud rates with timer 1 by leaving the timer 1 interrupt enabled, and configuring the timer to run as a 16-bit timer (high nibble of T01MOD = 0001b), and using the timer 1 interrupt to do a 16-bit embedded firmware reload. Note: the frequency fclk is the internal microcontroller frequency. If there is no clock divider then fclk = fosc.

For details on programming timer 1 to function as baud rate generator for the UART see Section 9.8 "TIMER 0/1 AND TIMER 2".

The next table lists the maximum baud rates for using mode 2 of timer 1.

Table 45: Maximum baud rates using mode 2 of timer 1

Reload Value	f_{CLK} divided by	SMOD	Baud Rate at f_{CLK}			Unit
			6.78	13.56	27.12	MHz
FF	96	1	70.6	141.2	282.5	kHz

The next table shows commonly used baud rates using mode 2 of timer 1 and a CLK frequency of 27.12 MHz.

Table 46: Baud rates using mode 2 of timer 1

Reload Value	f_{CLK} divided by	SMOD	Baud Rate at f_{CLK}	Unit
FC	706	0	38.4	kHz
F9	1412	0	19.2	kHz
F1	2825	0	9.6	kHz
E3	5650	0	4.8	kHz
C5	11300	0	2.4	kHz
8A	22600	0	1.2	kHz

9.7.5.2 Baud rates using timer 2 (UART mode 1 and 3)

The overflow output t2_ovf of the 80c51 timer2 module can be used to drive the UART input pin trigger2. The UART must be set in mode 1 or 3 and the input ttrigger2en must be 1 to select trigger2 for transmitting and the input rtrigger2en must be 1 to select trigger2 for receiving. Timer 2 has a programming mode to function as baud rate generator for the UART. In this mode the baud rate is given by formula:

$$\text{Baud Rate} = \frac{f_{clk}}{16 \times [65536 - (T2RCH, T2RCL)]}$$

When rewriting this formula, the value for the timer 2 reload values T2RCH/L is calculated from the desired baud rate as follows:

$$\text{Reload value T2RCH/L} = 65536 - \frac{f_{clk}}{16 \times Baudrate}$$

For details on programming timer 2 to function as baud rate generator for the UART see the timer 2 document. Note: the frequency fclk is the internal microcontroller frequency. If there is no clock divider then fclk = fosc.

The next table lists the maximum baud rates for using timer 2.

Table 47: Maximum baud rates using timer 2

Reload Value T2RCH/L	f_{CLK} divided by	Baud Rate at f_{CLK}			Unit
		6.78	13.56	27.12	MHz
FFFF	16	423	0.845	1.695	kHz

9.8 TIMER 0/1 AND TIMER 2

The TIMER 0/1 and Timer 2 are general purpose.

9.8.1 Feature list

The Timer 0/1 has the following functionality:

- Generate a wake-up request in response to an external interrupt (INT0 and/or INT1)
- External interrupt 0 and 1 edge and level detection
- Support Timer or Counter mode
- Support 4 operational modes

Timer 0/1 has two 16 bit registers which can operate either in a timer or a counter mode. These registers are identified as timer 0 and timer 1. Each of the timers can operate in one of four modes:

- Mode 0: a 13 bit timer/counter
- Mode 1: a 16 bit timer/counter
- Mode 2: an 8 bit timer/counter with programmable preload value
- Mode 3: two separate 8 bit timer/counters (timer 0 only)

The Timer 2 module implements enhanced timer 2 functionality:

The Timer 2 is a 16 bit timer/counter which can operate as either an event timer or an event counter in one of these four operating modes:

- Mode 0: capture
- Mode 1: auto-reload up/down counting
- Mode 2: baud rate generation
- Mode 3: clock output mode

9.8.2 TIMER 0/1 Functional Description

Timer 0/1 has two 16 bit registers which can operate either in a timer or a counter mode. These registers are identified as timer 0 and timer 1. Each of the timers can operate in one of four modes:

- Mode 0: a 13 bit timer/counter
- Mode 1: a 16 bit timer/counter
- Mode 2: an 8 bit timer/counter with programmable preload value
- Mode 3: two separate 8 bit timer/counters (timer 0 only)

In the “timer” function, the register is incremented every machine cycle. The count rate is 1/6 of the clock CLK frequency.

In the “counter” function, the register is incremented in response to a 1-to-0 transition at its input pin pad_t0 (timer 0) or pad_t1 (timer 1). The maximum count rate is 1/12 of the clock CLK frequency.

9.8.3 TIMER 0/1 embedded firmware View

The Timer 0/1 module has two 16-bit Timer/Counter registers: Timer 0 and Timer 1. Both can be configured as timers or event counters.

In the “timer” function, the register is incremented every machine cycle. The count rate is 1/6 of the clock CLK frequency.

In the “counter” function, the register is incremented in response to a 1-to-0 transition at its input pin pad_t0 (timer 0) or pad_t1 (timer 1). In this function the external input is sampled during CPU state 5 of every machine cycle. When the sample shows a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register in CPU state 3 of the machine cycle following the one in which the transition was detected. The maximum count rate is 1/12 of the clock CLK frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

In addition to the “timer” or “counter” selection, Timer 0 and Timer 1 have four operating modes from which to select. Both timer 0 and timer 1 modes can be chosen independently to each other, their modes need not be the same. However mode 3 has some exceptions.

The overflow output timer01_ovf1 of timer 1 can be used as a baud rate generator to drive the UART input pin trigger1. The timer 1 interrupt should be disabled in this application. In the most typical applications, when driving the UART, timer 1 is configured for ‘timer’ operation, in the auto-reload mode.

9.8.3.1 TIMER 0/1 Registers

The Timer 0/1 module contains six Special Function Registers (SFRs) that can be read and written by the CPU.

The embedded firmware reads in CPU state 5 and writes in CPU state 6
Through hardware, bits T01CON.TF0 and T01CON.TF1 are loaded during CPU state 2 and state 4 respectively. Through hardware, bits T01CON.IE0 and T01CON.IE1 are set during CPU state 1 and reset during state 2.
Through hardware registers T0L, T0H, T1L, T1H are updated during CPU state 1, 2, 3 and 4 respectively. In one machine cycle, the embedded firmware load overrides the hardware load.

Timer 0/1 Special Function Registers are listed in the following table.

Table 48: Timer 0/1 Special Function registers List

Name	Size [bytes]	Address Offset	Description	Access
T01CON	1	88h	Timer 0/1 control register	R/W
T01MOD	1	89h	Timer 0/1 mode register	R/W
T0L	1	8Ah	Timer 0 timer/counter low register	R/W
T1L	1	8Bh	Timer 1 timer/counter low register	R/W
T0H	1	8Ch	Timer 0 timer/counter high register	R/W
T1H	1	8Dh	Timer 1 timer/counter high register	R/W

9.8.3.2 Register T01CON

This Special Function Register is used to control the Timer 0/1.

Table 49: Timer 0/1 T01CON Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 50: Description ofTimer 0/1 T01CON Register bits

Bit	Symbol	Description
7	TF1	**Timer 1 overflow Flag.** Set by hardware on a timer 1 overflow.An active input iacktf1 delayed with two cycles clears the overflow flag (i.e. the interrupt is processed).
6	TR1	**Timer 1 Run control bit.** Set/cleared by embedded firmware only.When set the timer/counter 1 is turned on.When cleared the timer/counter 1 is turned off.
5	TF0	**Timer 0 overflow Flag.** Set by hardware on a timer 0 overflow.
4	TR0	**Timer 0 Run control bit.** Set/cleared by embedded firmware.When set the timer/counter is turned on.When cleared the timer/counter 0 is turned off.
3	IE1	**External Interrupt 1 Edge flag.** Set by hardware when an external interrupt is detected on INT1_N.
2	IT1	**External Interrupt 1 Type control bit.** Set/cleared by embedded firmware only.When set, interrupt 1 triggers on a falling edge of INT1_N. When cleared, interrupt 1 triggers on a low level of INT1_N.
1	IE0	**External Interrupt 0 Edge flag.** Set by hardware when an external interrupt is detected on INT0_N.
0	IT0	**External Interrupt 0 Type control bit.** Set/cleared by embedded firmware only.When set, interrupt 0 triggers on a falling edge of INT0_N. When cleared, interrupt 0 triggers on a low level of INT0_N.

9.8.3.3 Register T01MOD

This Special Function Register is used to configure the Timer 0/1.

Table 51: Timer 0/1 T01MOD Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
GATE1	C/T1	M11	M10	GATE0	C/T0	M01	M00

Table 52: Description of Timer 0/1 T01MOD Register bits

Bit	Symbol	Description
7	GATE1	**Timer 1 Gating control.** Set/cleared by embedded firmware only.When set, timer/counter 1 is enabled only when INT1_N is high and T01CON.TR1 is set.When cleared timer/counter 1 is enabled whenever T01CON.TR1 is set.The enable of timer/counter 1 is a boolean function: “INT1_N OR (NOT Gate) AND T01CON.TR1”.
6	C/T1	**Timer 1 or Counter 1 selector.** Set/cleared by embedded firmware only. When set, timer/counter 1 is set to counter operation.When cleared timer/counter 1 is set to timer operation.
5	M11	**Timer/counter 1 Mode.** Set/cleared by embedded firmware only. • Mode 0: – M11 = 0M10 = 08048 timer, T1L serves as a 5 bit prescaler. • Mode 1: – M11 = 0M10 = 116 bit timer/counter, T1H and T1L are cascaded. • Mode 2: – M11 = 1M10 = 08 bit auto reload timer/counter.T1H holds a value which is to be reloaded intoT1L each time T1L overflows. • Mode 3: – M11 = 1M10 = 1 Timer/counter 1 is stopped (it holds its count).
4	M10	
3	GATE0	**Timer 0 Gating control.** Set/cleared by embedded firmware only.When set, timer/counter 0 is enabled only when INT0_N is high and T01CON.TR0 is set.When cleared timer/counter 0 is enabled whenever T01CON.TR0 is set.The enable of timer/counter 0 is a boolean function: “INT0_N OR (NOT Gate) AND T01CON.TR0”
2	C/T0	**Timer 0 or Counter 1 selector.** Set/cleared by embedded firmware only. When set, timer/counter 0 is set to counter operation.When cleared timer/counter 0 is set to timer operation.
1	M01	**Timer/counter 0 Mode.** Set/cleared by embedded firmware only. • Mode 0: – M01 = 0M00 = 08048 timer, T0L serves as a 5 bit prescaler. • Mode 1: – M01 = 0M00 = 116 bit timer/counter, T0H and T0L are cascaded. • Mode 2: – M01 = 1M00 = 08 bit auto reload timer/counter.T0H holds a value which is to be reloaded intoT0L each time T0L overflows. • Mode 3: – M01 = 1M00 = 1 Timer/counter 0 is split into two 8 bit timer/counters, T0H and T0L. T0H is controlled bythe control bit of timer 0: T01CON.TR0. T0H iscontrolled by the standard timer 0 control: “INT0_N OR (NOT Gate0) ANDT01CON.TR0”.
0	M00	

9.8.3.4 Registers T0L, T0H

These two 8 bit registers are normal registers in the Special Function Register space. These are the actual timer/counter registers for timer 0. T0L is the least significant byte of timer/counter 0, T0H is the most significant byte of timer/counter 0.

Table 53: Timer 0/1 T0L Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
T0L.7	T0L.6	T0L.5	T0L.4	T0L.3	T0L.2	T0L.1	T0L.0

Table 54: Description of Timer 0/1 T0L Register bits

Bit	Symbol	Description
7 to 0	T0L.7 to T0L.0	Timer 0 timer/counter Least Significant Byte

Table 55: Timer 0/1 T0H Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
T0H.7	T0H.6	T0H.5	T0H.4	T0H.3	T0H.2	T0H.1	T0H.0

Table 56: Description of Timer 0/1 T0H Register bits

Bit	Symbol	Description
7 to 0	T0H.7 to T0H.0	Timer 0 timer/counter Most Significant Byte

9.8.3.5 Registers T1L, T1H

These two 8 bit registers are normal registers in the Special Function Register space. These are the actual timer/counter registers for timer 1. T1L is the least significant byte of timer/counter 1, T1H is the most significant byte of timer/counter 1.

Table 57: Timer 0/1 T1L Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
T1L.7	T1L.6	T1L.5	T1L.4	T1L.3	T1L.2	T1L.1	T1L.0

Table 58: Description of Timer 0/1 T1L Register bits

Bit	Symbol	Description
7 to 0	T1L.7 to T1L.0	Timer 1 timer/counter Least Significant Byte

Table 59: Timer 0/1 T1H Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
T1H.7	T1H.6	T1H.5	T1H.4	T1H.3	T1H.2	T1H.1	T1H.0

Table 60: Description of Timer 0/1 T1H Register bits

Bit	Symbol	Description
7 to 0	T1H.7 to T1H.0	Timer 1 timer/counter Most Significant Byte

9.8.3.6 Incrementer

The two 16-bit timer/counters are build around one eight-bits incrementer. The registers are incremented in the first four states, the overflow flags are set in state 2 and state 4.

- CPU state 1:
  - T0L is incremented if timer operation of timer/counter0 is active, or when a 1-to-0 transition is detected on pad_t0 input and counter operation is active.
- CPU state 2:
  - T0H is incremented if T0L overflows. The overflow flag T01CON.TF0 is updated.
- CPU state 3:
  - T1L is incremented if timer operation of timer/counter 1 is active, or when a 1-to-0 transition is detected on pad_t1 input and counter operation is active.
- CPU state 4:
  - T1H is incremented if T1L overflows. The overflow flag T01CON.TF1 is updated.

9.8.3.7 Overflow detection

An overflow is detected by comparing the incremented value of the most significant bit with its previous value. If the bit changed from 1 to 0, the register overflowed. An overflow detection of the lower byte register is clocked into a flip-flop and is used in the next state as the increment enable of the upper byte registers. An overflow detection of the upper byte registers will set the corresponding overflow bit in the T01CON register. The upper byte overflow is also clocked into a flip-flop to generate the output signals timer01_ovf0 and timer01_ovf1.

Overflow T01CON.TF0 is loaded during CPU state 2 and overflow T01CON.TF1 during CPU state 4. The interrupt controller of the 80C51 scans all requests at CPU state 2. Thus, an overflow of timer 0 or 1 is detected one cycle after it overflowed. Thereafter, if the request is serviced, the interrupt routine is called and the overflow flag is cleared. Execution of the interrupt routine starts in the fourth cycle after the timer overflowed. If in one cycle an overflow occurs and an acknowledge comes from the CPU, then the overflow flag is set. So a set overrules a reset. The timer01 receives the acknowledge from the CPU through inputs iacktf0 and iacktf1. The input iacktf1 is delayed with two cycles before clearing the overflow flag T01CON.TF1. The input iacktf0 is not delayed before clearing the overflow flag T01CON.TF0.

9.8.3.8 TIMER 0/1 Wake-up signal generation

The circuit can Wake-up from Power-down mode by a reset, but also by one of the two external interrupts. Wake-up from power-down by external interrupt 0/1 is only possible if T01CON.IE0/IE1 is enabled and level sensitive. Under these conditions, a low level on P32_int0 or P33_int1 will generate wake-up output signal timer01_wake.

9.8.4 TIMER 2 Functional Description

Timer2 can operate either as a timer or as an event counter. This is selected by bit T2CON.C/T2.

Timer2 can operate in one of four different modes: Capture mode, Auto-reload mode, Baud rate generation mode (for one or two UART) or Clock output mode. The four modes are selected by several bits of the T2CON and T2MOD registers.

Timer2 register values can change by hardware or by embedded firmware. In one machine cycle, the write by embedded firmware takes place in state 6 of the machine cycle. When in one machine cycle both an update by hardware and embedded firmware occurs in one of the registers T2H, T2L, RCAP2H or RCAP2L, the update by embedded firmware has precedence over the update by hardware. Each increment or decrement of timer2 occurs in state 1 except when in baud rate generation mode and configured as a counter. In this mode timer2 increments each clock cycle.

In the timer function u80c51_timer2 is incremented every machine cycle. Since a machine cycle consists of 6 clock periods, the count rate is 1/6 of the clock frequency. In the counter function, u80c51_timer2 is incremented in response to a 1-to-0 transition at its corresponding input *pad_t2*. Since it takes two machine cycles to recognize a 1-to-0 transition, the maximum count rate is 1/12 of the clock frequency.

9.8.5 TIMER 2 embedded firmware View

The Timer 2 module has extra bits in the T2CON and T2MOD registers to use as baudrate clock signals for the UART in the microcontroller.

Timer 2 can operate either as a timer or as an event counter. This is selected by bit T2CON.C/T2. Timer 2 can operate in one of four different modes: Capture mode, Auto-reload mode, Baud rate generation mode (for a UART) or Clock output mode. The four modes are selected by several bits of the T2CON and T2MOD registers. The four modes are described below.

9.8.5.1 TIMER 2 SFR Register List

Timer 2 has six Special Function Registers (SFR) that can be read and written by the CPU. These registers are: T2CON, T2MOD, T2H, T2L, RCAP2H and RCAP2L.

Timer 2 register values can change by hardware or by embedded firmware

In one machine cycle, the write by embedded firmware takes place in state 6 of the machine cycle.

When in one machine cycle both an update by hardware and embedded firmware occurs in one of the registers T2H, T2L, RCAP2H or RCAP2L, the update by embedded firmware has precedence over the update by hardware.

Each increment or decrement of timer 2 occurs in state 1 except when in baud rate generation mode and configured as a counter. In this mode timer 2 increments each clock cycle.

Table 61: Timer 2 SFR Register List

Name	Size [bytes]	SFR Address	Description	Access
T2CON	1	C8h	Timer 2 control register	R/W
T2MOD	1	C9h	Timer 2 mode register	R/W
RCAP2L	1	CAh	Timer 2 reload/capture low register	R/W
RCAP2H	1	CBh	Timer 2 reload/capture high register	R/W
T2L	1	CCh	Timer 2 timer/counter low register	R/W
T2H	1	CDh	Timer 2 timer/counter high register	R/W

9.8.5.2 Register T2CON

This Special Function register is used to control the TIMER 2.

Table 62: Timer 2 T2CON Register (address xxh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK0	TCLK0	EXEN2	TR2	C/T2	CP/RL2
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 63: Description of Timer 2 T2CON Register bits

Bit	Symbol	Description
7	TF2	**Timer 2 overflow Flag.** Set by a timer 2 overflow and must be cleared by embedded firmware.TF2 will not be set when baud rate generation mode, clock out mode or metalink mode is selected.
6	EXF2	**Timer 2 EXternal Flag.** Set on a negative transition on pad_t2ex and T2CON.EXEN2='1'.In auto-reload mode it is toggled on an under- or overflow (not in metalink mode,intd = 0).This bit must be cleared by embedded firmware.
5	RCLK0	**Timer 2 Receive CLocK UART flag.** Set by embedded firmware only.When set, it causes UART0 to use timer 2 overflow pulses.When reset, it causes UART0 to use overflow pulses from another source, for example timer 1 (in a standard configuration).
4	TCLK0	**Timer 2 Transmit CLocK UART flag.** Set by embedded firmware only.When set, it causes UART0 to use timer 2 overflow pulses.When reset, it causes UART0 to use overflow pulses from another source, for example timer 1 (in a standard configuration).
3	EXEN2	**Timer 2 EXternal ENable flag.** Set by embedded firmware only.When set, allows a capture or reload to occur, together with an interrupt, as a result of a negative transition on input pad_t2ex if in capture mode or auto reload mode with DCEN reset.If in auto reload mode and DCEN is set, the EXEN2 bit has no influence.In the other modes EXF2 is set and an interrupt is generated on a 1 to 0 transition on T2EX pin. When EXEN2 is reset, timer 2 ignores events at pad_t2ex in all modes.
2	TR2	**Timer 2 Run control.** Set by embedded firmware only.When set, the timer is started. When reset the timer is stopped.
1	C/T2	**Timer 2 Counter/Timer selector.** Set by embedded firmware only.When set the counter function is selected, when reset the timer function is selected.
0	CP/RL2	**Timer 2 CaPture/ReLoad flag.** Set by embedded firmware only.Selection of mode capture or reload.When set the capture function is selected, when reset the reload function is selected. When baud rate generation mode is selected this bit is ignored and timer 2 is forced to auto-reload on an overflow.

9.8.5.3 Register T2MOD

This Special Function Register is used to select TIMER2 mode.

Table 64: Timer 2 T2MOD Register (address xxh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	RCLK1	TCLK1	-	T2RD	T2OE	DCEN
Reset	X	X	0	0	X	0	0	0
Access	-	-	R/W	R/W	-	R	R/W	R/W

Table 65: Description of Timer 2 TMOD Register bits

Bit	Symbol	Description
7 to 6	-	Reserved; not implemented.
5	RCLK1	**Timer 2 Receive CLocK UART1 flag.** Set by embedded firmware only. When set, it causes UART1 to use timer 2 overflow pulses.When reset, it causes UART1 to use overflow pulses from another source, for example timer 1 (in a standard configuration).
4	TCLK1	**Timer 2 Transmit CLocK UART1 flag.** Set by embedded firmware only. When set, it causes UART1 to use timer 2 overflow pulses.When reset, it causes UART1 to use overflow pulses from another source, for example timer 1 (in a standard configuration).
3	-	**Reserved; not implemented.**
2	T2RD	**Timer 2 ReaD flag.** Set/reset by hardware and embedded firmware.This bit is set by hardware if a T2L read operation is followed by an increment of T2H before a T2H read operation.This bit is reset on the trailing edge of next T2L read.This bit is used to indicate that the16 bit timer 2 register is not read properly since the T2H part was incremented by hardware before it was read.
1	T2OE	**Timer 2 Output Enable bit.** Set by embedded firmware only.When set and T2CON.TF2 is reset and T2CON.EXF2 is reset, output timer2_t2 outputs a clock signal. When this condition is not met, output timer2_t2 outputs a logic ‘1’.The clock output is half the overflow frequency of timer 2.
0	DCEN	**Timer 2 Down Count ENable flag.** Set by embedded firmware only. When this bit is set and input pad_t2ex is set timer 2 can be configured (in auto_reload mode) as an up counter. When this bit is reset or input pad_t2ex is reset, timer 2 can be configured (in auto-reload mode) as a down counter.

9.8.5.4 Registers T2L, T2H

They are the actual timer/counter registers.

On the fly reading can give a wrong value since T2H can be changed after T2L is read and before T2H is read. This situation is indicated by flag T2RD in T2MOD.

In all cases the two 8 bit registers operate as one 16 bit timer/counter register.

Table 66: Timer 2 T2L Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
T2L.7	T2L.6	T2L.5	T2L.4	T2L.3	T2L.2	T2L.1	T2L.0

Table 67: Description of Timer 2 T2L Register bits

Bit	Symbol	Description
7 to 0	T2L.7 to T2L.0	Timer 2 timer/counter Least Significant Byte

Table 68: Timer 2 T2H Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
T2H.7	T2H.6	T2H.5	T2H.4	T2H.3	T2H.2	T2H.1	T2H.0

Table 69: Description of Timer 2 T2H Register bits

Bit	Symbol	Description
7 to 0	T2H.7 to T2H.0	Timer 2 timer/counter Most Significant Byte

9.8.5.5 Registers RCAP2L, RCAP2H

They are the capture and reload registers depending on the chosen operation mode.

In the capture mode the RCAP2H/RCAP2L registers are loaded with the value of the T2H/T2L registers.

In the reload mode the T2H/T2L registers are loaded with the value of the RCAP2H/RCAP2L registers.

Table 70: Timer 2 RCAP2L Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Table 71: Description of Timer 2 RCAP2L Register bits

Bit	Symbol	Description
7 to 0	RCAP2L.7 to RCAP2L.0	Timer 2 capture/reload Least Significant Byte

Table 72: Timer 2 RCAP2H Register (address xxxxh) bit allocation, reset value: 0000_0000h

7	6	5	4	3	2	1	0
RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Table 73: Description of Timer 2 RCAP2H Register bits

Bit	Symbol	Description
7 to 0	RCAP2H.7 to RCAP2H.0	Timer 2 capture/reload Least Significant Byte

9.9 IOs configuration and Miscellaneous registers

The ConfigI0_I1 register is used to select the host interface for communication.

Table 74: Config IO_I1 Register (address 6103h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	int1_pol	-	pad_I1	-	pad_I0	enselif	Selif	
Reset	0	0	X	0	X	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 75: Description of Config IO_I1 Register bits

Bit	Symbol	Description
7	int1_pol	**Configure the polarity of the INT1 interrupt.** When set to 0, the value the p33_int1 pin is not inverted. When set to 1, the value the p33_int1 pin is inverted.
6	-	Reserved.
5	pad_I1	When read this bit give the state of the I1 pin.
4	-	Reserved.
3	pad_I0	When read this bit give the state of the I0 pin.
2	enselif	When set to 1, this bit indicates that the selif bits are valid and that the selected interface on the MATX can drive the pins. When set to 0, the MATX cannot drive the IO lines.
1 to 0	Selif	These bits are used by the embedded firmware to select the host interface communication link. see Table 88 “HOST interface selection” on page 72.

The Observe_testbus register can be used for system integration and trouble shooting.

Table 76: Observe_testbus Register (address 6104h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	usb_main_clock	-	-	-	-	-	-	observe_cluart
Reset	0	X	X	X	X	X	X	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 77: Description of Observe_testbus Register bits

Bit	Symbol	Description
7	usb_main_clock	Configure the RST_OUT pin to observe USB main clockWhen set to 0, the RST_OUT pin shows the system reset. When set to 1, the RSTOUT pin shows the USB main clock signal.
6 to 1	-	Reserved.
0	observe_cluart	Configure the pads P30, P31, P32, P33, P34, P35 to observe internal cluart data bus. When set to 0, the pads have the default functions. When set to 1, the pads are configured in output mode and show the internal data_bus of the cluart.

Table 78: Data_rng Register (address 6105h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	data_rng							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 79: Description of Data_rng Register bits

Bit	Symbol	Description
7 to 0	data_rng	Random number data register.

The control_rngpower register can be used to control the rng behaviour or the regulator.

Table 80: Control_rngpower Register (address 6106h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	hide_svdd_sig	sam_switch_overload	sam_switch_en	curlimoff	cpu_need_rng	random_dataready	vdd_ok
Reset	X	X	0	0	X	0	0	0
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

Table 81: Description of Control_rngpower Register bits

Bit	Symbol	Description
7	-	Reserved.
6	hide_svdd_sig	**Configure the internal state of the input signal of SIGIN and P34 in an idle state.** This bit can be used to avoid spikes on SIGIN and P34 when the SVDD switch becomes enabled or disabled. When set to 0, the internal state of SIGIN and P34 signals are driven by respectively the pads SIGIN and P34. When set to 1, the internal state of SIGIN is fixed to 0 and the internal state of P34 is fixed to 1.
5	sam_switch_overload	**This bit indicates the state of the current limitation of the SVDD switch.** When set to 0, it indicates that the current consumption into the SVDD switch does no exceed the limit. When set to 1, the current limitation of the SVDD switch is activated by the switch.
4	sam_switch_en	**This bit is used to enable or disable the power on the SVDD switch.** When set to 0, the SVDD switch is disabled and the SVDD output power is discharge to the ground. When set to 1, the SVDD switch is enabled and the SVDD output deliver power to the SAM and to the internal pads (SIGIN, SIGOUT and P34).
3	curlimoff	**Configure the regulator to deliver more current than 100 mA.** When set to 0, the 100 mA current limitations is activated. When set to 1, the 100 mA current limitations is desactivated.
2	cpu_need_rng	**Force the random number generator in running mode**. When set to 0, the random number generator is under control of the cluart. When set to 1, the random number generator is forced to run.
1	random_dataready	**Indicates availability of random number.** When set to 0, it indicates that a new random number is not available. It is automatically set to 0 when the register data_rng is read When set to 1, it indicates that a new random number is available.
0	vdd_ok	**This signal indicates that the VDD supplied by the regulator is OK.** When set to 0, the regulator has not reached the nominal voltage to switch off the current limitation of the regulator. When set to 1, it indicates that the regulator output reachs the nominal voltage and that the current limitation can be switched off.

The gpirq register can be used to control the general purpose interrupt.

Table 82: Gpirq Register (address 6107h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	gpirq_level_P71	gpirq_level_P50	gpirq_level_P35	gpirq_level_P34	gpirq_enable_P71	gpirq_enable_P50	gpirq_enable_P35	gpirq_enable_P34
Reset	X	1	0	0	0	0	0	0
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

Table 83: Description of Gpirq Register bits

Bit	Symbol	Description
7	gpirq_level_P71	**This bit is used to control the level of P71 (MISO) to generate an interrupt on the GPIRQ interrupt source (and wake-up event if enabled).** When set to 0, an interrupt will be generated if P71 is at level “0” and if gpirq_enable_P71 is set to 1. When set to 1, an interrupt will be generated if P71 is at level “1” and if gpirq_enable_P71 is set to 1.
6	gpirq_level_P50	**This bit is used to control the level of P50 (NSS) to generate an interrupt on the GPIRQ interrupt source (and wake-up event if enabled).** When set to 0, an interrupt will be generated if P50 is at level “0” and if gpirq_enable_P50 is set to 1. When set to 1, an interrupt will be generated if P50 is at level “1” and if gpirq_enable_P50 is set to 1.
5	gpirq_level_P35	**This bit is used to control the level of P35 to generate an interrupt on the GPIRQ interrupt source (and wake-up event if enabled).** When set to 0, an interrupt will be generated if P35 is at level “0” and if gpirq_enable_P35 is set to 1. When set to 1, an interrupt will be generated if P34 is at level “1” and if gpirq_enable_P35 is set to 1.
4	gpirq_level_P34	**This bit is used to control the level of P34 to generate an interrupt on the GPIRQ interrupt source (and wake-up event if enabled).** When set to 0, an interrupt will be generated if P34 is at level “0” and if gpirq_enable_P34 is set to 1. When set to 1, an interrupt will be generated if P34 is at level “1” and if gpirq_enable_P34 is set to 1. If hide_svdd_sig is set to 1 and gpirq_enable_P34 is also set to 1 then GPIRQ will be asserted independently of the level on the pad P34.
3	gpirq_enable_P71	When set to 1, enables the pad P71 (MISO) to generate an interrupt on the GPIRQ interrupt source (IRQ number 14) according to the state of the gpirq_level_P71 bit.
2	gpirq_enable_P50	When set to 1, enables the pad P50 (NSS) to generate an interrupt on the GPIRQ interrupt source (IRQ number 14) according to the state of the gpirq_level_P50 bit.
1	gpirq_enable_P35	When set to 1, enables the pad P35 to generate an interrupt on the GPIRQ interrupt source (IRQ number 14) according to the state of the gpirq_level_P35 bit.
0	gpirq_enable_P34	When set to 1, enables the pad P34 to generate an interrupt on the GPIRQ interrupt source (IRQ number 14) according to the state of the gpirq_level_P34 bit.

9.9.1 General purpose IO PORTs

The general purpose IO ports are configured in 1 or several controllable modes. At maximum 4 different embedded firmware controllable modes can be supported. Port 3 is configured in Quasi Bidirectional mode only except for P3[4] which support the 4 configurable modes. P5 is configured in Open Drain mode only. Port 7 supports the 4 configurable modes. The port 7 is configurable thought the P7CFGA and P7CFGB registers. The supported configuration modes are the following:

- P7CFGA[n]=0 and P7CFGB[n]=0: Open drain
- P7CFGA[n]=1 and P7CFGB[n]=0: Quasi Bidirectional (Reset mode)
- P7CFGA[n]=0 and P7CFGB[n]=1: input (High Impedance)
- P7CFGA[n]=1 and P7CFGB[n]=1: Push/pull output

- P3CFGA[4]=0 and P3CFGB[4]=0: Open drain
- P3CFGA[4]=1 and P3CFGB[4]=0: Quasi Bidirectional (Reset mode)
- P3CFGA[4]=0 and P3CFGB[4]=1: input (High Impedance)
- P3CFGA[4]=1 and P3CFGB[4]=1: Push/pull output

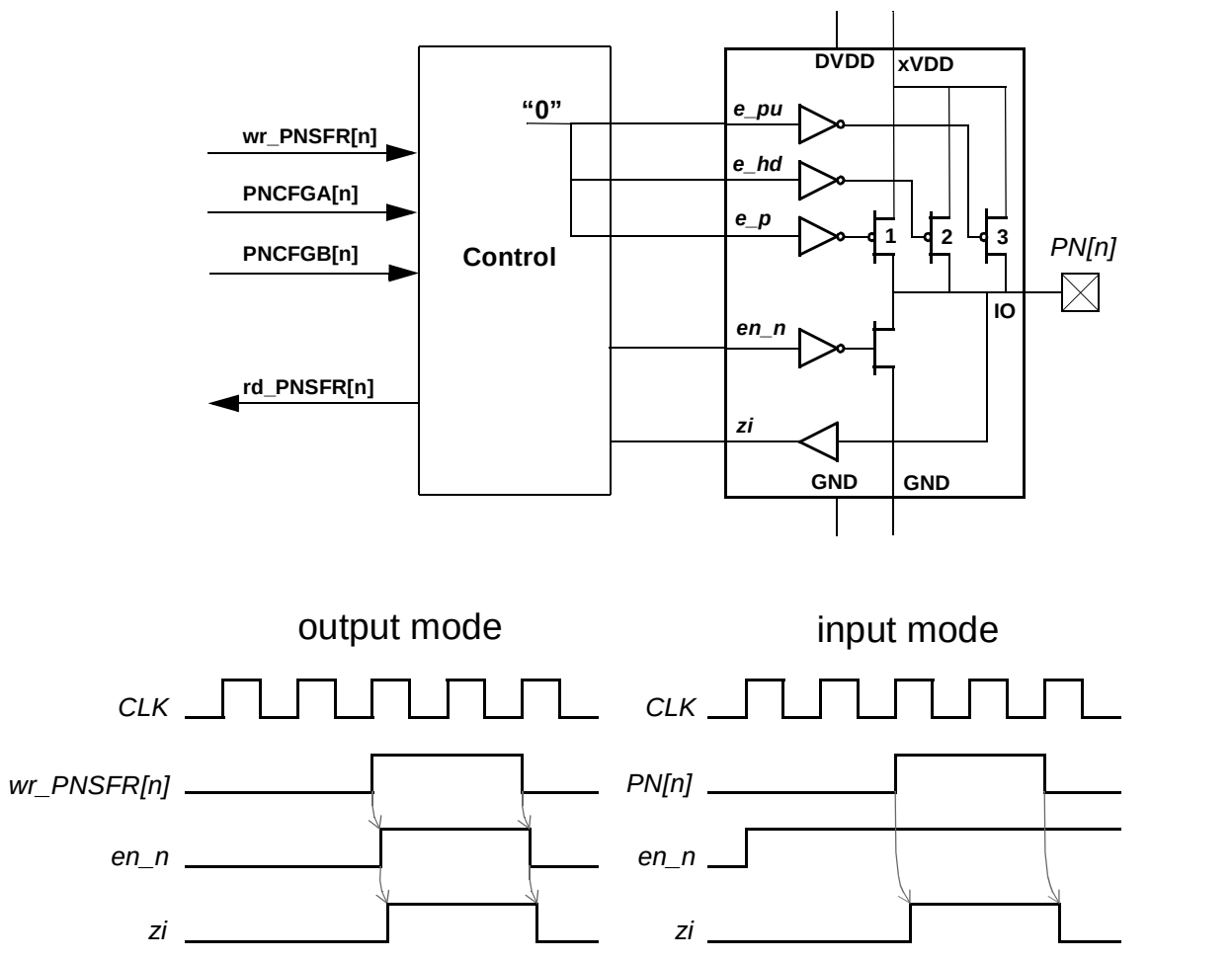


Fig 22. Open Drain

In open drain configuration, an external pull-up resistor is required to output or read a logic ‘1’. When wr_PNSFR[n] is ‘0’ the pad cell pin is pulled down to ‘0’. When wr_PNSFR[n] is ‘1’ the pad cell pin is High Impedant.

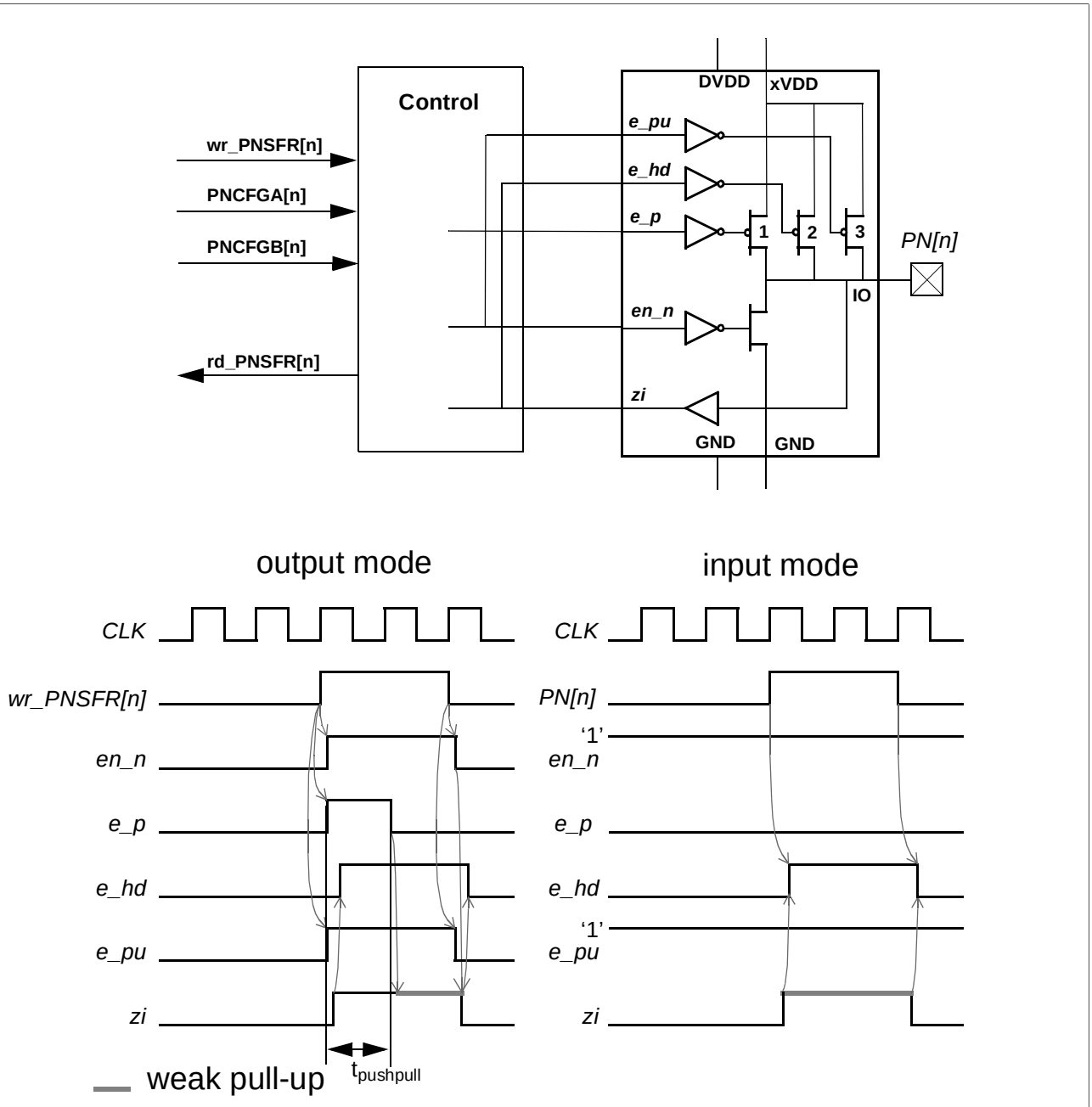


Fig 23. Quasi Bidirectional

In Quasi Bidirectional configuration, e_p is driven to ‘1’ for only one CLK period on a low to high transition of wr_PNSFR[n]. During the $t_{pushpull}$ time the pad drive a strong ‘1’ at its output. On the following CPU clock cycle this state will be held by the weak hold transistor which implements a latch function. Because of the weaker nature of this hold transistor, the pad cell can now act as an input as well. A third very weak pull up transistor ensures that an open input is read as ‘1’.

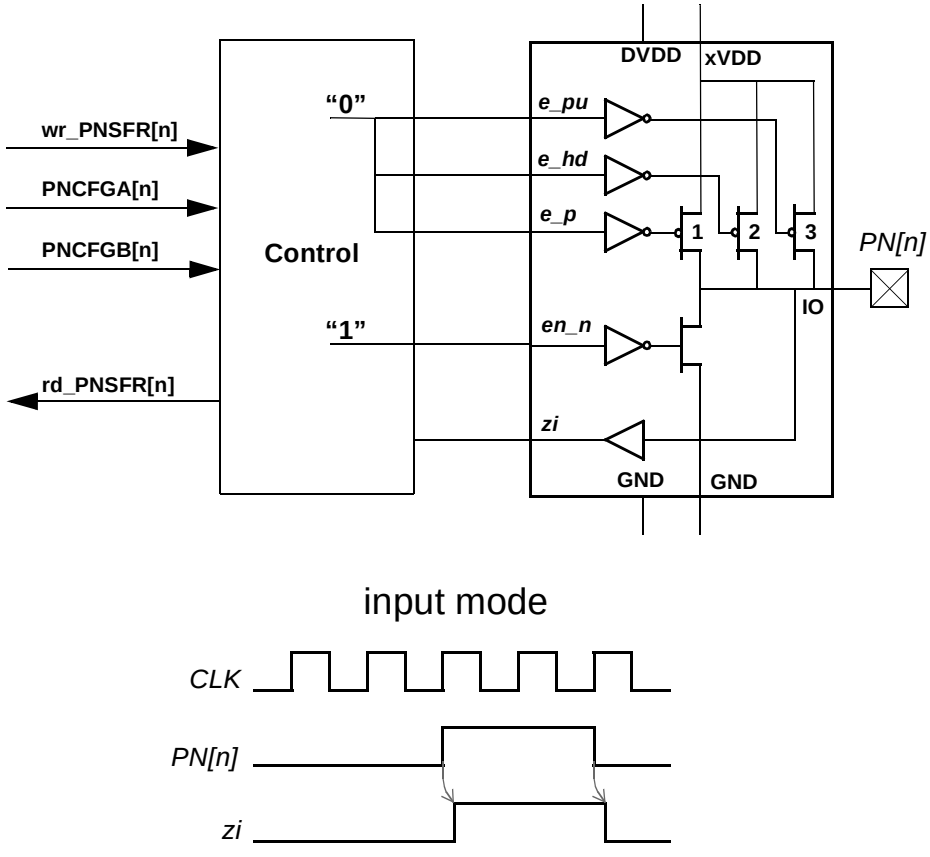


Fig 24. Input

In input configuration, no pull up or hold resistor are internally connected to the pad.

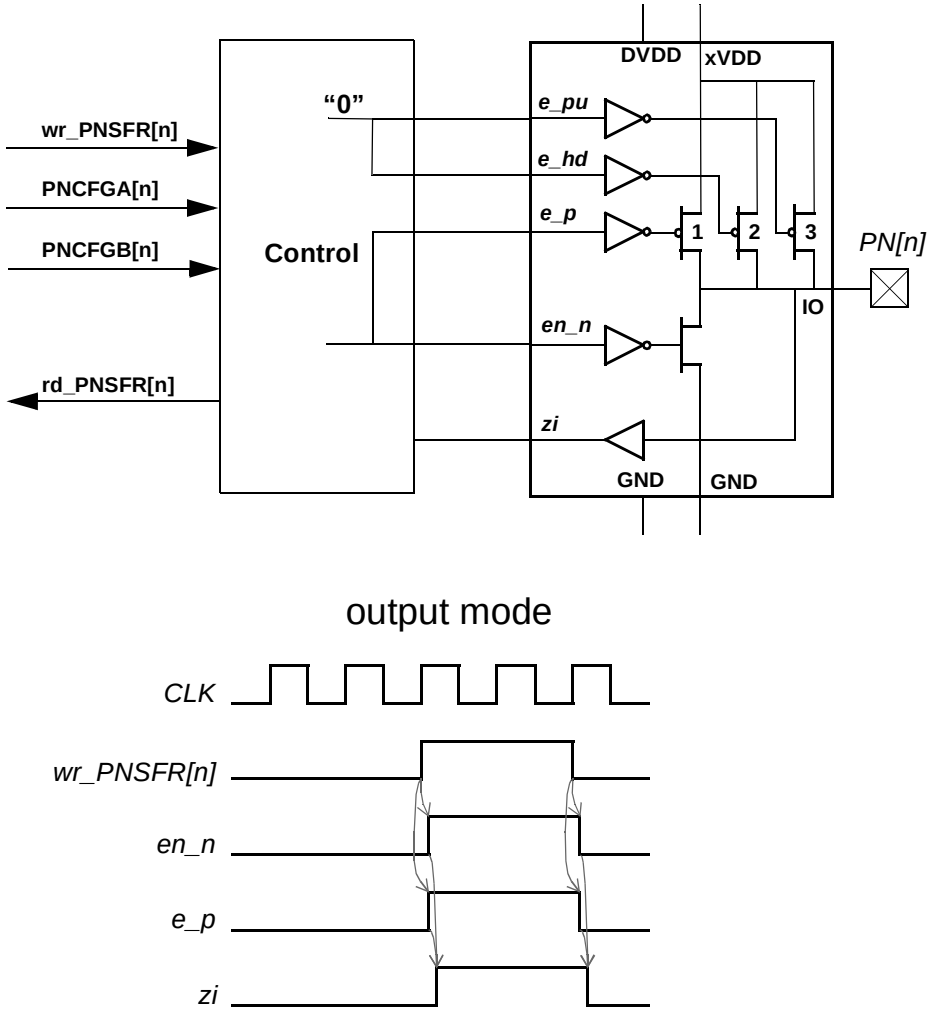


Fig 25. Push/Pull Output

In Push/pull configuration, the output pin drives a strong '0' or a '1' continuously, and input is impossible. It is possible to read back the pin output value.

Table 84: P7CFGA (SFR: address F4h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	P7CFGA(2)	P7CFGA(1)	P7CFGA(0)
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 85: Description of P7CFGA Register bits

Bit	Symbol	Description
7 to 3	P7CFGA	Reserved.
2	P7CFGA(2)	In conjuction with P7CFGB, it configures the functional mode of P72 of the SCK MATX pin (Refer to Table 81 “HOST interface selection”) according to the mode defined in Section 9.9.1 “General purpose IO PORTs”.
1	P7CFGA(1)	In conjuction with P7CFGB, it configures the functional mode of P71 of the MISO MATX pin according to the mode defined in Section 9.9.1 “General purpose IO PORTs”.
0	P7CFGA(0)	In conjuction with P7CFGB, it configures the functional mode of IRQ pin according to the mode defined in Section 9.9.1 “General purpose IO PORTs”.

Table 86: P7CFGB Register (SFR: address F5h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	P7CFGB(2)	P7CFGB(1)	P7CFGB(0)
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 87: Description of P7CFGB Register bits

Bit	Symbol	Description
7 to 3	P7CFGB	Reserved.
2	P7CFGB(2)	In conjuction with P7CFGA, it configures the functional mode of P72 of the SCK MATX pin (Refer to Table 81 “HOST interface selection”) according to the mode defined in Section 9.9.1 “General purpose IO PORTs”.
1	P7CFGB(1)	In conjuction with P7CFGA, it configures the functional mode of P71 of the MISO MATX pin according to the mode defined in Section 9.9.1 “General purpose IO PORTs”.
0	P7CFGB(0)	In conjuction with P7CFGA, it configures the functional mode of IRQ pin according to the mode defined in Section 9.9.1 “General purpose IO PORTs”.

Table 88: P7 Register (SFR: address F7h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	P7C(2)	P7C(1)	P7C(0)
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 89: Description of P7 Register bits

Bit	Symbol	Description
7 to 3	P7C	Reserved.
2	P7C(2)	Writing to P7(2) writes the corresponding value to the P72 pin according to the configuration mode defined by P7CFGA(0) and P7CFGB(0). Reading from P7(0) reads the state of P72 pin.
1	P7C(1)	Writing to P7(1) writes the corresponding value to the P71 pin according to the configuration mode defined by P7CFGA(0) and P7CFGB(0). Reading from P7(0) reads the state of P71 pin.
0	P7C(0)	Writing to P7(0) writes the corresponding value to the IRQ pin according to the configuration mode defined by P7CFGA(0) and P7CFGB(0). Reading from P7(0) reads the state of IRQ pin.

Table 90: P5 Register (SFR: address D7h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	P5(1)	P5(0)
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 91: Description of P5 Register bits

Bit	Symbol	Description
7 to 2	P5C	Reserved.
1	P5C(1)	Writing to P5(1) writes the corresponding value to SDA of the MOSI MATX pin (Refer to Table 81 “HOST interface selection”) according to the open drain configuration mode. Reading from P5(0) reads the state of MOSI MATX pin.
0	P5C(0)	Writing to P5(0) writes the corresponding value to SCL of the NSS MATX pin (Refer to Table 81 “HOST interface selection”) according to the open drain configuration mode. Reading from P5(0) reads the state of NSS MATX pin.

Table 92: P3CFGA Register (SFR: address FCh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	P3CFGA(4)	-	-	-	
Reset	1	1	1	1	1	1	1	1
Access	R	R	R	R/W	R	R	R	R

Table 93: Description of P3CFGA Register bits

Bit	Symbol	Description
7 to 5		Reserved.
4	P3CFGA(4)	In conjuction with P3CFGB(4), it configures the functional mode of P34.
3 to 0		Reserved.

Table 94: P7CFGB Register (SFR: address FDh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	P3CFGB(4)	-	-	-	
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R	R	R

Table 95: Description of P7CFGB Register bits

Bit	Symbol	Description
7 to 5		Reserved.
4	P3CFGB(4)	In conjuction with P3CFGA(4), it configures the functional mode of P34.
3 to 0		Reserved.

Table 96: P3 Register (SFR: address B0h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	P3(5)	P3(4)	P3(3)	P3(2)	P3(1)	P3(0)
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 97: Description of P3 Register bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5	P3(5)	Writing to P3(5) writes the corresponding value to P35 pin according to the Quasi Bidirectional mode. Reading from P3(5) reads the state of P35 pin.
4	P3(4)	When SAMclk_p34_en (Refer to Table 189 “CL UART SAMClk_en Register”) is set to 0, writing to P3(4) writes the corresponding value to P34 pin according to the configuration mode defined by P3CFGA(4) and P3CFGB(4). Reading from P3(4) reads the state of P34 pin.
3	P3(3)	Writing to P3(3) writes the corresponding value to P33 pin according to the Quasi Bidirectional mode. Reading from P3(3) reads the state of P33 pin.
2	P3(2)	Writing to P3(2) writes the corresponding value to P32 pin according to the Quasi Bidirectional mode. Reading from P3(2) reads the state of P32 pin.
1	P3(1)	When the P31 alternate function is not used (Uart_tx pin), writing to P3(1) writes the corresponding value to P31 pin according to the Quasi Bidirectional mode. Reading from P3(1) reads the state of P31 pin.
0	P3(0)	When the P30 alternate function is not used (Uart_rx pin), writing to P3(0) writes the corresponding value to P30 pin according to the Quasi Bidirectional mode. Reading from P3(0) reads the state of P30 pin.

9.10 HOST INTERFACES

PN531 must be able to support different kind of interfaces to communicate with the HOST. All the interface that have to be supported are exclusive.

9.10.1 Feature list

- USB 2.0 full speed Device interface compliant
- SPI interface compliant
- I^2C interface compliant
- High speed RS232 interface compliant

9.10.2 Host interface Block Diagram

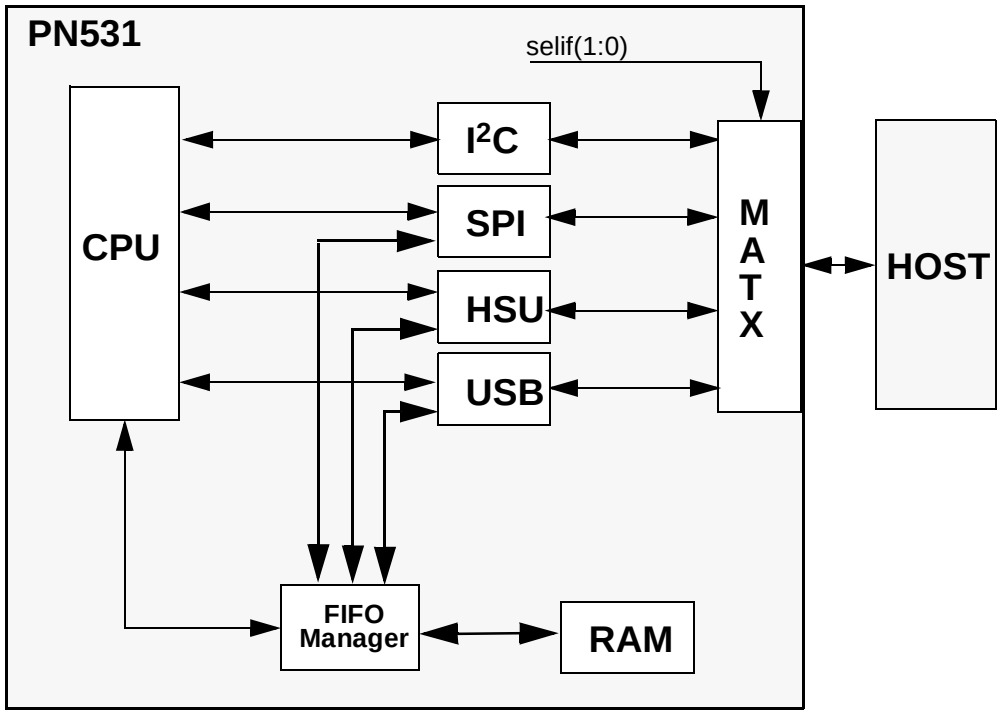


Fig 26. Host interface Block diagram

9.10.3 MATX short description

General Overview

After every Power-On or Hard Reset (RSTPD at high level), the PN531 also resets its interfaces and checks the current HOST interface type.

The PN531 identifies the selected HOST interface by means of the logic levels on the control pins I0 and I1 after the Reset Phase. This is done by a combination of fixed pin connections

The Power for the MATX is delivered from PVDD.

Table 98: HOST interface selection

PN531 Pin number	Config_IO_I1 register selif[1] selif[0]	Host Interface selected			
		HSU	I^2C	SPI	USB
31	NSS	RX	SCL (P50)	NSS	D+
32	MOSI	TX	SDA (P51)	MOSI	D-
33	MISO	P71	P71	MISO	P71
34	SCK	P72	P72	SCK	P72

9.10.4 Host interface Functional Description

- Overview: The PN531 is able to support a SPI interface, an USB 2.0 full speed Device interface, an I^2C interface and also a serial UART interface supporting specific high baudrates.
- FIFO: To optimize the data flow (baudrates) between the HOST and the CPU, a FIFO is used. This FIFO is shared between the interfaces and cannot be used concurrently. Then, FIFO manager block control the dataflows with the different interfaces and the RAM memory. The size of the fifo is 182 bytes.
  - The RAM used as a FIFO is divided into two part: A receive part and a transmit part. A dedicated address will be defined for each of these 2 FIFOs.
  - The common part between the SPI and high speed UART interface sharing the FIFO is the FIFO manager block. It consists of a Data register, a Status register and also some registers to define the characteristics of the FIFO (ex: size, waterlevel). These registers are addressed by the CPU through SFRs.
- The size of the fifo is 182 bytes
- The following Figure 28 “Registers management Block diagram.” on page 74 describes how is managed the registers repartition between the FIFO manager, the SPI, the high speed UART interfaces or the USB.

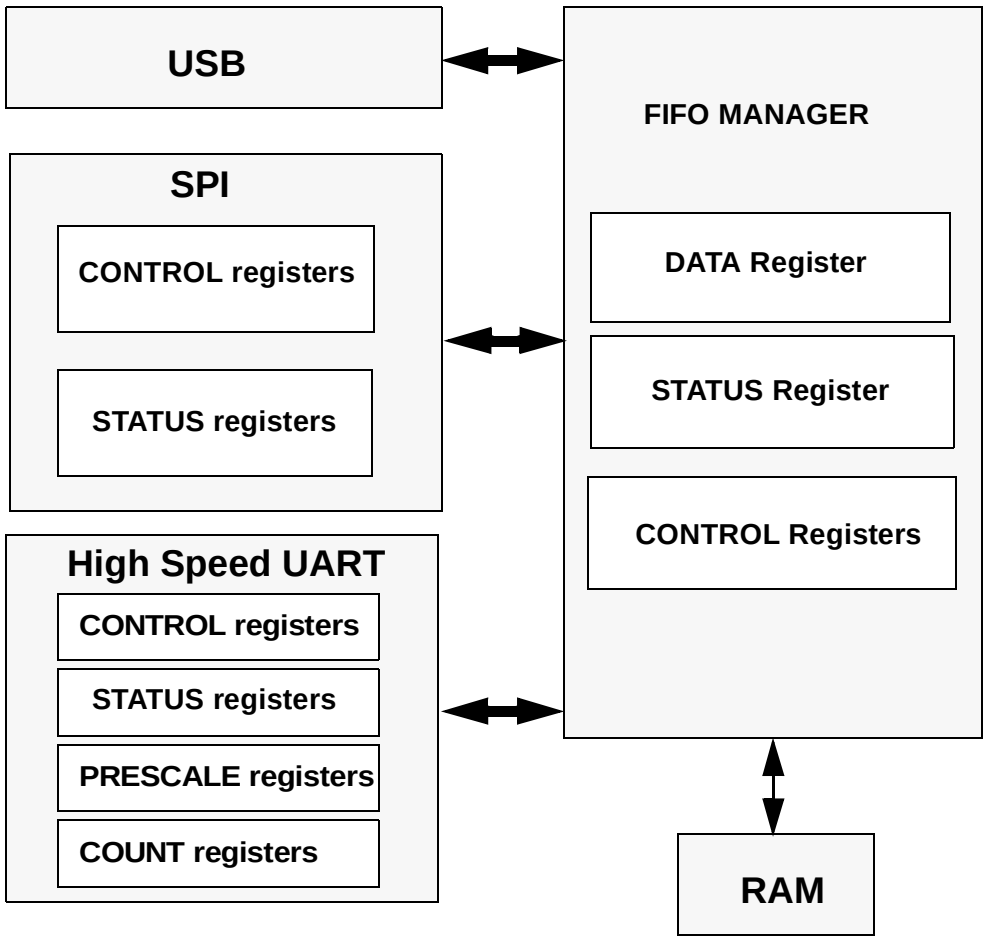


Fig 27. Registers management Block diagram

9.10.5 FIFO MANAGER

9.10.5.1 Feature list

- Configuration of the FIFO (size, waterlevel ...)
- Management of received and transmit data exchanged with High Speed UART, SPI and CPU interfaces.
- Interrupt generation going to the CPU

9.10.5.2 FIFO manager Block Diagram

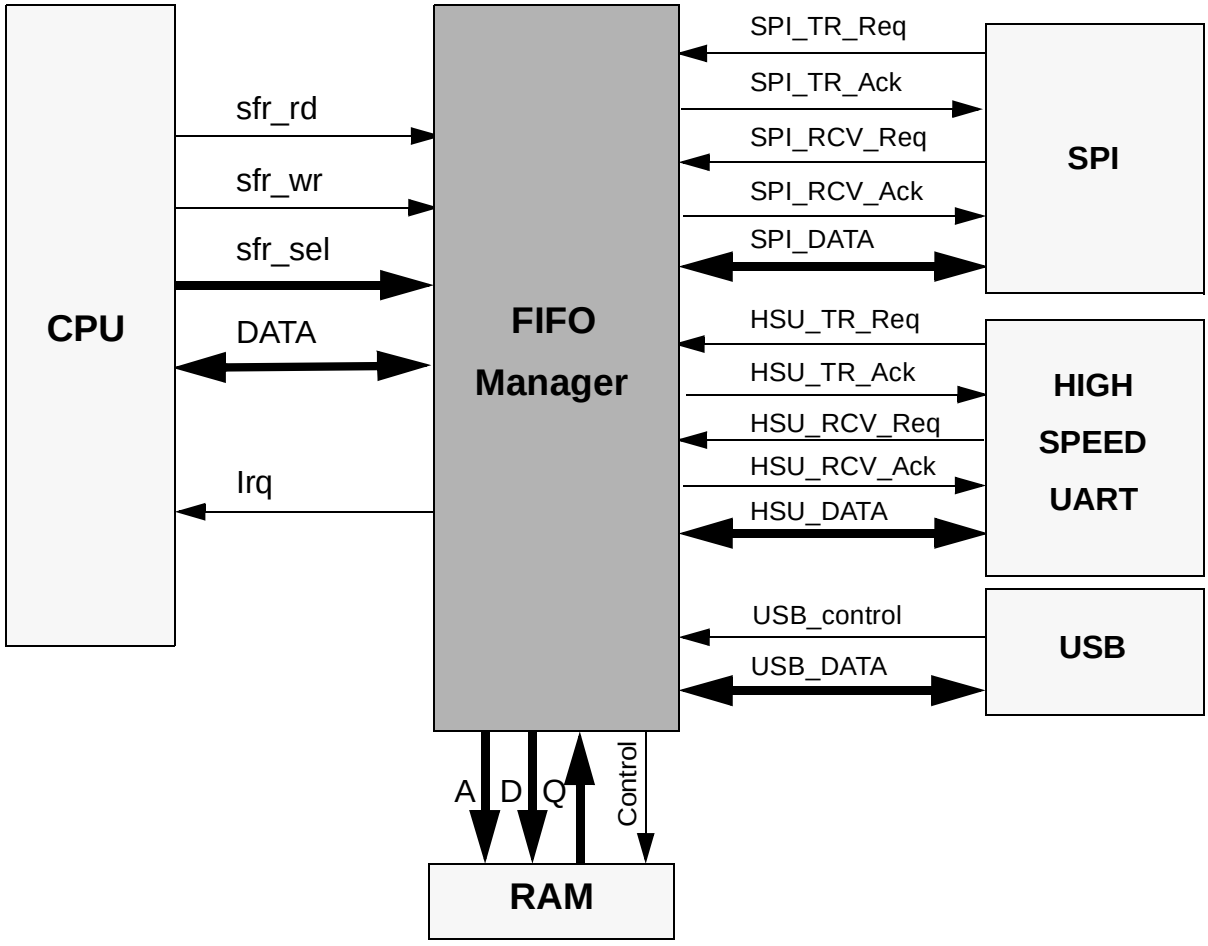


Fig 28. FIFO manager Block diagram

9.10.5.3 FIFO manager Functional Description

- **Overview:** This block is designed to manage a Ram as a FIFO in order to optimize the data exchange between the CPU and the HOST.
- **Sharing:** This RAM is shared between the USB, SPI and High Speed UART interfaces. Indeed, these interfaces cannot be used simultaneously. The selection of the interface used is done by embedded firmware. The FIFO manager block is the common part between the USB, the SPI and the HSU interfaces. It consists of a Data register, a Status register and also some registers to define the characteristics of the FIFO. These registers are addressed by the CPU.
- **Reception/Transmission:** The RAM used as a FIFO is divided into two part: A receive part and a transmit part. A dedicated address will be defined for each of these 2 FIFOs.
- **Conflict:** This block also manages the possible conflicts existing around the FIFO between the CPU and the interfaces. Indeed, a request coming from the interface (TR_req or RCV_req) can be simultaneous with a request to access to the data register coming from the CPU.

9.10.5.4 FIFO manager SFR Register List

9 registers are needed to manage the FIFO manager.

Table 99: Fifo Manager SFR Register List

Name	Size [bytes]	SFR Address	Description	Access
FITEN	1	A1h	Interrupt Enable and Reset FIFO	R
FDATA	1	A2h	Data reception/transmission buffer	R/W
FSIZE	1	A3h	Control the size of the FIFO in Reception and in transmission	R/W
RWL	1	9Ah	FIFO Receive Waterlevel: Control the waterlevel of the FIFO in reception	R/W
TWL	1	9Bh	FIFO Transmit Waterlevel: Control the waterlevel of the FIFO in transmission	R/W
FIFOFS	1	9Ch	FIFO Transmit FreeSpace: Controls the number of characters which can still be loaded in the FIFO	R/W
FIFOFF	1	9Dh	FIFO Receive Fullfilment:Control the number of received characters in the FIFO	R/W
SFF	1	9Eh	Global Status/Error messages	R
FIT	1	9Fh	Interrupt Source	R/W

9.10.5.5 TWL Register

This register defines the warning level of the transmit FIFO for the CPU. It implies a FIFO buffer underflow.

Table 100: TWL Register (SFR: address 9Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TWaterlevel							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 101: Description of TWL Register bits

Bit	Symbol	Description
7 to 0	TWaterlevel	Level of fulfillment to set a warning

9.10.5.6 RWL Register

This register defines the warning level of the receive FIFO for the CPU. It implies a FIFO buffer overflow.

Table 102: RWL Register (SFR: address 9Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RWaterlevel							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 103: Description ofRTWL Register bits

Bit	Symbol	Description
7 to 0	RWaterlevel	Level of fulfillment to set a warning

9.10.5.7 FSIZE

This register defines the size of the FIFO in reception. The maximum size is 180 bytes. The free space not used by the receive FIFO in the RAM will be allocated to Transmit FIFO.

Table 104: FSIZE Register (SFR: address A3h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Receive size							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 105: Description of FSIZE Register bits

Bit	Symbol	Description
7 to 0	Receive size	Size of the Receive FIFO

9.10.5.8 FIFOFS

This register defines the number of characters that the CPU can still load into the FIFO until the transmit FIFO is full.

Table 106: FIFOFS Register (SFR: address 9Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Transmit freespace							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 107: Description of FIFOFS Register bits

Bit	Symbol	Description
7 to 0	Transmit freespace	Freespace FIFO

9.10.5.9 FIFOFF

This register defines the number of characters already received and loaded into the receive FIFO.

Table 108: FIFOFF Register (SFR: address 9Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Receive fulfillment							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 109: Description of FIFOFF Register bits

Bit	Symbol	Description
7 to 0	Receive fulfillment	Size of the Receive FIFO

9.10.5.10 SFF Register

The status register is byte addressable. It contains read-only bits which are used to allow the CPU to monitor the status of the FIFO. The primary purpose of this register is to detect completion of a data transfers.

Table 110: SFF Register (SFR: address 9Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFO_EN	-	TWLL	TFF	TFE	RWLH	RFF	RFE
Reset	0	-	1	0	1	0	0	1
Access	R/W	-	R	R	R	R	R	R

Table 111: Description of SFF Register bits

Bit	Symbol	Description
7	FIFO_EN	**Fifo Enable:** Set to 1 this bit enables the fifo manager clock (CPU_CLK), set to 0 the clock remains low.
6	-	Reserved.
5	TWLL	**Transmit WaterlLevelLow:** This bit is set to 1 when the number of bytes stored into the transmit fifo is equal or smaller than the transmit TWaterlevel.
4	TFF	**Transmit FIFO Full:** This is set to 1 if the transmitted part of the FIFO is full. It is cleared when a transfer is completed.
3	TFE	**Transmit FIFO Empty:** This bit indicates when the transmitted part of the FIFO is empty. This bit is set to 0 when the CPU writes a character in the data register.
2	RWLH	**Receive WaterLevel High**: This bit is set to 1 when the number of bytes stored into the received fifo is greater or equal to the RWaterlevel.
1	RFF	**Receive FIFO Full:** This bit is set to 1 in the receive part of the FIFO is full. It is cleared by reading the data register.
0	RFE	**Receive FIFO Empty:** This bit indicates when the receive part of the FIFO is empty. It is set to 0 when a data transfer is completed. This bit is cleared by reading the data register until there is no character anymore in the received FIFO.

9.10.5.11 FIT Register

The Interrupt register is byte addressable. It contains read-write bits which generate the interrupt going to the CPU. This interrupt is a OR-ed of all these bits.

Table 112: FIT Register (SFR: address 9Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Reset	-	WCOL_IRQ	TWLL_IRQ	TFF_IRQ	RWLH_IRQ	ROVR_IRQ	RFF_IRQ
Reset	1	0	0	1	0	0	0	0
Access	W	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 113: Description of FIT Register bits

Bit	Symbol	Description
7	Reset	**Reset:** Set to 1, Reset defines that the marked bits in this register are set. Set to 0, Reset defines that the marked bits in this register are cleared.
6	-	Reserved, for future use.
5	WCOL_IRQ	**Write COLlision IRQ:** This bit is set to 1 when the transmitted part of the FIFO is already full (TFF is set to 1) and a new character is written by the CPU in the data register.It is cleared thanks to bit reset (20h).
4	TWLL_IRQ	**Transmit WaterlLevelLow IRQ:** This bit is set to 1 when equal or less than the transmit waterlevel bytes are in the transmit FIFO. It is cleared thanks to bit reset (10h).
3	TFF_IRQ	**Transmit FIFO Full:** This is set to 1 if the transmitted part of the FIFO is full. It is cleared thanks to bit reset (08h).
2	RWLH_IRQ	**Receive WaterLevel High IRQ:** This bit is set to 1 if the renaming FIFO receive space is equal or less than Waterlevel bytes in the buffer. It is cleared thanks to bit reset (04h).
1	ROVR_IRQ	**Read OVeRrun IRQ:** This bit indicates that a read overrun has occured.It occurs when the receiver part of the FIFO is full and a new data transfer is completed. Then the new received data is lost and ROVR_IRQ is set. It is cleared thanks to bit reset (02h).
0	RFF_IRQ	**Receive FIFO Full IRQ:** This bit is set to 1 if the received part of the FIFO is full. It is cleared by using the reset bit; so writing 01h in this register.

9.10.5.12 FITEN Register

The FITEN control register is byte addressable. It enables or disables the passing of interrupt requests. It is also used to reset the content of the receive FIFO.

Table 114: FITEN Register (SFR: address A1h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TFLUSH	RFLUSH	EN_WCOL_IRQ	EN_TWLL_IRQ	EN_TFF_IRQ	EN_RWLH_IRQ	EN_ROVR_IRQ	EN_RFF_IRQ
Reset	0	0	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 115: Description of FITEN Register bits

Bit	Symbol	Description
7	TFLUSH	This bit is set to 1 to reset the pointer of the transmit FIFO.
6	RFLUSH	This bit is set to 1 to reset the pointer of the receive FIFO.
5	EN_WCOL_IRQ	**Enable Write COLlision IRQ:** This bit is set to 1 when the WCOL_IRQ is enable, else it is disabled.
4	EN_TWLL_IRQ	**Enable Transmit WaterlLevelLow IRQ:** This bit is set to 1 when the TWLL_IRQ is enable, else it is disabled.
3	EN_TFF_IRQ	**Enable Transmit FIFO Full:** This is set to 1 when the TFF_IRQ is enable, else it is disabled.
2	EN_RWLH_IRQ	**Enable Receive WaterLevel High IRQ:** This bit is set to 1 when the RWLH_IRQ is enable, else it is disabled.
1	EN_ROVR_IRQ	**Enable Read OVeRrun IRQ:** This bit is set to 1 when the ROVR_IRQ is enable, else it is disabled.
0	EN_RFF_IRQ	**Enable Receive FIFO Full IRQ:** This bit is set to 1 when the RFF_IRQ is enable, else it is disabled.

9.10.5.13 FDATA Register

The FDATA register is byte addressable. It is used to provide the transmit and receive data bytes. Each data written in the data register is push into the transmit FIFO. Each data read from the data register is pop from the receive FIFO.

Table 116: FDATA Register (SFR: address A2h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FDATA							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 117: Description of FDATA Register bits

Bit	Symbol	Description
7 to 0	FDATA	Writing to FDATA writes to the transmit buffer. Reading from FDATA reads from the receive buffer.

9.11 I²C Interface

The I²C module implements a master/slave I²C bus interface with integrated shift register, shift timing generation and slave address recognition. It is compliant to the I²C bus specification IC20/Jan. 92. I²C standard mode (100 kHz SCLK) and fast mode (400 kHz SCLK) are supported.

9.11.1 Feature list

The mains characteristics of the I²C module are:

- Support master/slave I²C bus
- Standard and fast mode supported

The I²C module is control through few registers (I²C0CON, I²C0DAT, I²C0STA, I²C0ADR).

9.11.2 I²C Functional Description

The I²C interface may operate in any of the following four modes:

- Master Transmitter
- Master Receiver
- Slave Receiver
- Slave Transmitter

As a master, the I²C logic will generate all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the I²C bus will not be released.

Two types of data transfers are possible on the I²C bus:

- Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
- Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows the data bytes transmitted by the slave to the master. The master returns an acknowledge bit after each received byte except the last byte. At the end of the last received byte, a “not acknowledge” is returned.

In a given application, SIO1 may operate as a master and as a slave. In the slave mode, the SIO1 hardware looks for its own slave address and the general call address. If one of these addresses is detected, an interrupt is requested. When the microcontroller wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave action is not interrupted. If bus arbitration is lost in the master mode, SIO1 switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

9.11.3 Master Transmitter Mode

Serial data is output through SDA while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7-bit SLA) and the data direction bit. In this case the data direction bit (R/W) will be a logic ‘0’ (W). Serial data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

In the master transmitter mode, a number of data bytes can be transmitted to the slave receiver. Before the master transmitter mode can be entered, I^2C0CON must be initialized with the ENS1 bit set and the STA, STO and SI bits reset. ENS1 must be set to enable the SIO1 interface. If the AA bit is reset, SIO1 will not acknowledge its own slave address or the general call address if they are present on the bus. This will prevent the SIO1 interface from entering a slave mode.

The master transmitter mode may now be entered by setting the STA bit. The SIO1 logic will then test the I^2C bus and generate a start condition as soon as the bus becomes free. When a START condition is transmitted, the serial interrupt flag (SI) is set, and the status code in the status register (I^2C0STA) will be 08H. This status code must be used to vector to an interrupt service routine that loads I^2C0DAT with the slave address and the data direction bit (SLA+W). The SI bit in I^2C0CON must then be reset before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in I^2C0STA are possible. The appropriate action to be taken for any of the status codes is detailed in the table. After a repeated start condition (state 10H), SIO1 may switch to the master receiver mode by loading I^2C0DAT with SLA+R.

9.11.4 Master Receiver Mode

The first byte transmitted contains the slave address of the transmitting device (7-bit SLA) and the data direction bit. In this case the data direction bit (R/W) will be logic 1 (R). Serial data is received via SDA while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

In the master receiver mode, a number of data bytes are received from a slave transmitter. The transfer is initialized as in the master transmitter mode. When the START condition has been transmitted, the interrupt service routine must load I^2C0DAT with the 7-bit slave address and the data direction bit (SLA+R). The SI bit in I^2C0CON must then be cleared before the serial transfer can continue.

When the slave address and the data direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes are possible in I^2C0STA. The appropriate action to be taken for each of the status codes is detailed in the table. After a repeated start condition (state 10H), SIO1 may switch to the master transmitter mode by loading I^2C0DAT with SLA+W.

9.11.5 Slave Receiver Mode

Serial data and the serial clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

In the slave receiver mode, a number of data bytes are received from a master transmitter. To initiate the slave receiver mode, I^2C0ADR must be loaded with the 7-bit slave address to which SIO1 will respond when addressed by a master. Also the least significant bit of I^2C0ADR should be set if the interface should respond to the general call address (00H). The control register, I^2C0CON, should be initialized with ENS1 and AA set and STA, STO, and SI reset in order to enter the slave receiver mode. Setting the AA bit will enable the logic to acknowledge its own slave address or the general call address and ENS1 will enable the interface.

When I^2C0ADR and I^2C0CON have been initialized, SIO1 waits until it is addressed by its own slave address followed by the data direction bit which must be ‘0’ (W) for SIO1 to operate in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag (SI) is set and a valid status code can be read from I^2C0DAT. This status code should be used to vector to an interrupt service routine, and the appropriate action to be taken for each of the status codes is detailed in the table. The slave receiver mode may also be entered if arbitration is lost while SIO1 is in the master mode.

If the AA bit is reset during a transfer, SIO1 will return a not acknowledge (logic ‘1’) to SDA after the next received data byte. While AA is reset, SIO1 does not respond to its own slave address or a general call address. However, the I^2C bus is still monitored and address recognition may be resumed at any time by setting AA. This means that the AA bit may be used to temporarily isolate SIO1 from the I^2C bus.

9.11.6 Slave Transmitter Mode

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via SDA while the serial clock is input through SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

In the slave transmitter mode, a number of data bytes are transmitted to a master receiver. Data transfer is initialized as in the slave receiver mode. When I^2C0ADR and I^2C0CON have been initialized, SIO1 waits until it is addressed by its own slave address followed by the data direction bit which must be ‘1’ (R) for SIO1 to operate in the slave transmitter mode. After its own slave address and the R bit have been received, the serial interrupt flag (SI) is set and a valid status code can be read from I^2C0STA. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status codes is detailed in the table. The slave transmitter mode may also be entered if arbitration is lost while SIO1 is in the master mode.

If the AA bit is reset during a transfer, SIO1 will transmit the last byte of the transfer and enter state C0H or C8H. SIO1 is switched to the not addressed slave mode and will ignore the master receiver if it continues the transfer. Thus the master receiver receives all ‘1’s as serial data. While AA is reset, SIO1 does not respond to its own slave address or a general call address. However, the I^2C bus is still monitored, and address recognition may be resumed at any time by setting AA. This means that the AA bit may be used to temporarily isolate SIO1 from the I^2C bus.

9.11.7 I²C SFR register list

Table 118: I²C SFR Register List

Name	Size [bytes]	SFR Address	Description	Access
I²C0CON	1	D8h	Control register	R/W
I²C0STA	1	D9h	Status register	R/W
I²C0DAT	1	DAh	Data register	R/W
I²C0ADR	1	DBh	Slave Address register	R/W

9.11.7.1 I²C0CON Register

The CPU can read from and write to this 8-bit SFR. Two bits are affected by the Serial IO (SIO1) hardware: the SI bit is set when a serial interrupt is requested, and the STO bit is cleared when a STOP condition is present on the I²C bus. The STO bit is also cleared when ENS1 = ‘0’.

Table 119: FSIZE Register (SFR: address A3h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CR(2)	ENS1	STA	STO	SI	AA	CR(1:0)	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 120: Description of FSIZE Register bits

Bit	Symbol	Description
7	CR(2)	S**erial clock frequency selection in master mode.** These three bits determine the Clock Rate (serial clock frequency) when SIO1 is in a master mode. Special attention has to be made on the I2C bit frequency in case of dynamic switching of the CPU clock frequency.
6	ENS1	**Serial IO enable bit.** When Serial IO enable bit is ‘0’, the I²C_sda and I²C_scl outputs are constantly at 1 level leading to a high impedance state at the associated port lines SDA and SCL. The state of the SDA and SCL input lines pad_sda and pad_scl is ignored, SIO1 is in the “not addressed” slave state, and the STO bit in I²C0CON is forced to ‘0’. No other bits are affected. SDA and SCL port lines may be used as open drain I/O ports. When ENS1 is ‘1’, SIO1 is enabled. The port latches associated to SDA and SCL must be set to logic 1. ENS1 should not be used to temporarily release SIO1 from the I²C bus since, when ENS1 is reset, the I²C bus status is lost. The AA flag should be used instead.
5	STA	**START flag.** When the START bit is set to enter a master mode, the SIO1 hardware checks the status of the I²C bus and generates a START condition if the bus is free. If the bus is not free, then SIO1 waits for a STOP condition (which will free the bus) and generates a START condition after a delay of a half clock period of the internal serial clock generator. If STA is set while SIO1 is already in a master mode and one or more bytes are transmitted or received, SIO1 transmits a repeated START condition. STA may be set at any time. STA may also be set when SIO1 is an addressed slave. When the STA bit is reset, no START condition or repeated START condition will be generated.
4	STO	**STOP flag.** When the STOP bit is set while SIO1 is in a master mode, a STOP condition is transmitted to the I²C bus. When the STOP condition is detected on the bus, the SIO1 hardware clears the STO flag. In a slave mode, the STO flag may be set to recover from an error condition. In this case, no STOP condition is transmitted to the I²C bus. However, the SIO1 hardware behaves as if a STOP condition has been received and switches to the defined “not addressed” slave receiver mode. The STO flag is automatically cleared by the hardware. If the STA and STO bits are both set, the STOP condition is transmitted to the I²C bus if SIO1 is in a master mode (in a slave mode, SIO1 generates an internal STOP condition which is not transmitted). SIO1 then transmits a START condition. When the STO bit is reset, no STOP condition will be generated.

Table 120: Description of FSIZE Register bits *...continued*

Bit	Symbol	Description
3	SI	**Serial interrupt flag.** When the Serial Interrupt flag is set, then, if the serial interrupt from the SIO1 port is enabled, the CPU will receive an interrupt. SI is set by hardware when any one of 25 of the possible 26 SIO1 states are entered.The only state that does not cause SI to be set is state F8H, which indicates that no relevant state information is available. While SI is set, the low period of the serial clock on the SCL line is stretched, and the serial transfer is suspended. A high level on the SCL line is unaffected by the serial interrupt flag. SI must be reset by embedded firmware. When the SI flag is reset, no serial interrupt is requested, and there is no stretching of the serial clock on the SCL line.
2	AA	**Assert Acknowledge flag.** If the Assert Acknowledge flag is set, an acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when: • The “own slave address” has been received. • The general call address has been received while the general call bit (GC) in I^2C0ADR is set. • A data byte has been received while SIO1 is in the master receiver mode. • A data byte has been received while SIO1 is in the addressed slave receiver mode. When SIO1 is in the addressed slave transmitter mode, state C8H will be entered after the last serial bit is transmitted. When SI is cleared, SIO1 leaves state C8H, enters the not addressed slave receiver mode, and the SDA line remains at a high level. In state C8H, the AA flag can be set again for future address recognition. When SIO1 is in the not addressed slave mode, its own slave address and the general call address are ignored. Consequently, no acknowledge is returned, and a serial interrupt is not requested. Thus, SIO1 can be temporarily released from the I^2C bus while the bus status is monitored. While SIO1 is released from the bus, START and STOP conditions are detected, and serial data is shifted in. Address recognition can be resumed at any time by setting the AA flag. If the AA flag is set when the part’s own slave address or the general call address has been partly received, the address will be recognized at the end of the byte transmission.
1	CR(1:0)	**Serial clock frequency selection in master mode.**
0		

Table 121: I^2C CR(2:0) field description

CR2	CR1	CR0	CPU_CLK divided by	I^2C bit frequency according to CPU_clk
0	0	0	10	CPU_CLK/10
0	0	1	20	CPU_CLK/20
0	1	0	30	CPU_CLK/30
0	1	1	40	CPU_CLK/40
1	0	0	80	CPU_CLK/80
1	0	1	120	CPU_CLK/120
1	1	0	160	CPU_CLK/160
1	1	1	(256-T1 reload value)*12 24 ... 3072	CPU_CLK/3072 ... CPU_CLK/24

9.11.7.2 I²C0DAT Register

I²C0DAT contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from and write to this 8-bit SFR while it is not in the process of shifting a byte. This occurs when SIO1 is in a defined state and the serial interrupt flag is set. Data in I²C0DAT remains stable as long as SI is set. Data in I²C0DAT is always shifted from right to left: the first bit to be transmitted is the MSB (bit 7), and, after a byte has been received, the first bit of received data is located at the MSB of I²C0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in; I²C0DAT always contains the last data byte present on the bus. Thus, in the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data in I²C0DAT.

Table 122: I²C0DAT Register (SFR: address D9h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SD(7:0)							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 123: Description of I²C0DAT Register bits

Bit	Symbol	Description
7 to 0	SD(7:0)	Serial Data

Eight bits to be transmitted or just received. A logic ‘1’ in I²C0DAT corresponds to a high level on the I²C bus, and a logic ‘0’ corresponds to a low level on the bus. Serial data shifts through I²C0DAT from right to left.

I²C0DAT and the ACK flag form a 9-bit shift register which shifts in or shifts out an 8-bit byte, followed by an acknowledge bit. The ACK flag is controlled by the SIO1 hardware and cannot be accessed by the CPU. Serial data is shifted through the ACK flag into I²C0DAT on the rising edges of clock pulses on the SCL line. When a byte has been shifted into I²C0DAT, the serial data is available in I²C0DAT, and the acknowledge bit is returned by the control logic during the ninth clock pulse. Serial data is shifted out from I²C0DAT via a buffer on the falling edges of clock pulses on the SCL line.

When the CPU writes to I²C0DAT, the buffer is loaded with the contents of I²C0DAT(7) which is the first bit to be transmitted to the SDA line. After nine serial clock pulses, the eight bits in I²C0DAT will have been transmitted to the SDA line, and the acknowledge bit will be present in ACK. Note that the eight transmitted bits are shifted back into I²C0DAT.

9.11.7.3 I²C0STA Register

I²C0STA is an 8-bit read-only special function register. The three least significant bits are always zero. The five most significant bits contain the status code. There are 26 possible status codes. When I²C0STA contains F8H, no relevant state information is available and no serial interrupt is requested. Reset initializes I²C0STA to F8H. All other I²C0STA values correspond to defined SIO1 states. When each of these states is entered, a serial interrupt is requested (SI = ‘1’), this can happen in any CPU cycle, and a valid status code will be present in I²C0STA. This status code will remain present in I²C0STA until SI is cleared by embedded firmware.

Note that I²C0STA changes one clock cycle after SI changes, so the new status can be visible in the same machine cycle SI changes or possibly (in one out of six cases) the machine cycle after that. This should not be a problem since you should not read I²C0STA before either polling SI or entry of the interrupt handler (which in itself takes several machine cycles).

Table 124: I²C0STA Register (SFR: address DAh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ST(7:0)							
Reset	F8h	F8h	F8h	F8h	F8h	F8h	F8h	F8h
Access	R	R	R	R	R	R	R	R

Table 125: Description of I²C0STA Register bits

Bit	Symbol	Description
7 to 0	ST(7:0)	**Encoded status bit for the different functional mode.** Several Status codes are returned in a certain mode (master transmitter, master receiver, slave transmitter, slave receiver) plus some miscellaneous status codes that can be returned at any time.

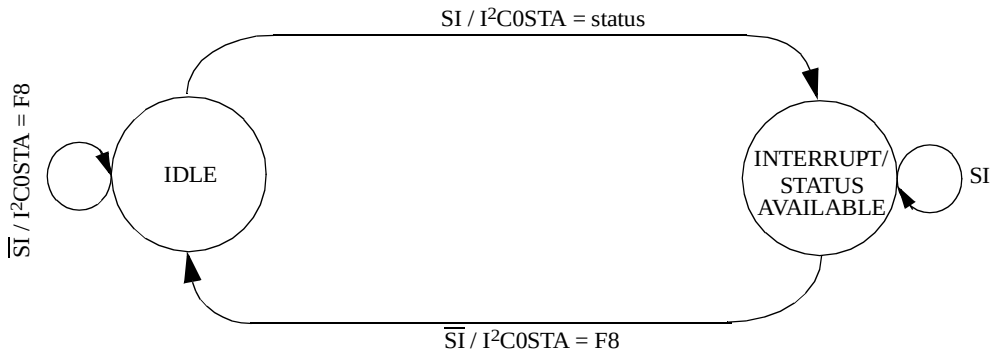


Fig 29. I²C State Machine of status behavior

Table 126: I²C Master Transmitter Mode status code

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
08H	A START condition has been transmitted	Load SLA+W	X	0	0	X	SLA+W will be transmitted ACK will be received
10H	A repeated START condition has been transmitted	Load SLA+W or Load SL+R	X	0	0	X	As above
			X	0	0	X	SLA+W will be transmitted; SIO1 will be switched to MST/(TRX or REC) mode
18H	SLA+W has been transmitted; ACK has been received	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received
			1	0	0	X	Repeated START will be transmitted;
		no I²C0DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
		no I²C0DAT action or no I²C0DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset
20H	SLA+W has been transmitted; NOT ACK has been received	Load data byte or	0	0	0	X	Data bye will be transmitted; ACK bit will be received
			1	0	0	X	Repeated START will be transmitted;
		no I²C0DATI²C0DATI²C0DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
		no I²C0DAT action or no I²C0DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset

Table 126: I²C Master Transmitter Mode status code *…continued*

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
28H	Write data byte in I²C0DAT has been transmitted; ACK has been received	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received
			1	0	0	X	Repeated START will be transmitted;
		no I²C0DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
		no I²C0DAT action or no I²C0DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset
30H	Write data byte in I²C0DAT has been transmitted; NOT ACK has been received	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received
			1	0	0	X	Repeated START will be transmitted;
		no I²C0DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
		no I²C0DAT action or no I²C0DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset
38H	Arbitration lost in SLA+R/W or Data bytes	No I²C0DAT action or	0	0	0	X	I²C bus will be released; a slave mode will be entered
		No I²C0DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free

Table 127: I²C Master Receiver Mode status codes

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
08H	A START condition has been transmitted	Load SLA+W	X	0	0	X	SLA+W will be transmitted ACK will be received
10H	A repeated START condition has been transmitted	Load SLA+W or Load SL+R	X	0	0	X	As above
			X	0	0	X	SLA+W will be transmitted; SIO1 will be switched to MST/(TRX or REC) mode
38H	Arbitration lost in SLA+R/W or Data bytes	No I²C0DAT action or	0	0	0	X	I²C bus will be released; a slave mode will be entered
		No I²C0DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free
40H	SLA+R has been transmitted; ACK has been received	No I²C0DAT action or	0	0	0	0	Data byte will be received; NOT ACK bit will be returned
		no I²C0DAT action	0	0	0	1	Data byte will be received; ACK bit will be returned

Table 127: I²C Master Receiver Mode status codes *...continued*

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
48H	SLA+R has been transmitted; NOT ACK has been received	No I²C0DAT action or	1	0	0	X	Repeated START condition will be transmitted
		no I²C0DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
		no I²C0DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset
50H	Read data byte has been received; ACK has been returned	Read data byte or	0	0	0	0	Data byte will be received; NOT ACK bit will be returned
		read data byte	0	0	0	1	Data byte will be received; ACK bit will be returned
58H	Read data byte has been received; NOT ACK has been returned	Read data byte or	1	0	0	X	Repeated START condition will be transmitted
		read data byte or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
		read data bye	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset

Table 128: I²C Slave Receiver Mode status codes

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
60H	Own SLA+W has been received; ACK has been returned	No I²C0DAT action or	X	0	0	0	Data byte will be received an NOT ACK will be returned
		no I²C0DAT action	X	0	0	1	Data bye will be received and ACK will be returned
68H	Arbitration lost in SLA+R/W as master; Own SLA+W has been received, ACK returned	No I²C0DAT action or	X	0	0	0	Data byte will be received an NOT ACK will be returned
		no I²C0DAT action	X	0	0	1	Data byte will be received and ACK will be returned
70H	General call address (00H) has been received; ACK has been returned	No I²C0DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		no I²C0DAT action	X	0	0	1	Data byte will be received and ACK will be returned
78H	Arbitration lost in SLA+R/W as master; General call address has been received, ACK has been returned	No I²C0DAT action or	X	0	0	0	Data byte will be received an NOT ACK will be returned
		no I²C0DAT action	X	0	0	1	Data byte will be received and ACK will be returned

Table 128: I²C Slave Receiver Mode status codes *…continued*

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
80H	Previously addressed with own SLA; Write data byte has been received; ACK has been returned	Read data byte or	X	0	0	0	Data byte will be received an NOT ACK will be returned
		read data byte	X	0	0	1	Data byte will be received and ACK will be returned
88H	Previously addressed with own SLA; Write data byte has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		read data byte	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'
		read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'. A START condition will be transmitted when the bus becomes free

Table 128: I²C Slave Receiver Mode status codes *...continued*

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
90H	Previously addressed with General Call; Write data byte has been received; ACK has been returned	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		read data byte	X	0	0	1	Data byte will be received and ACK will be returned
98H	Previously addressed with General Call; Write data byte has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		read data byte	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'
		read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'. A START condition will be transmitted when the bus becomes free
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/(REC or TRX)	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		read data byte	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'
		read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'. A START condition will be transmitted when the bus becomes free

Table 129: I²C Slave Transmitter Mode status codes

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
A8H	Own SLA+R has been received; ACK has been returned	Load data bye or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received
B0H	Arbitration lost in SLA+R/W as master; Own SLA+R has been received. ACK has been returned	Load data bye or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received
B8H	Read data bye in I²C0DAT has been transmitted; ACK has been received	Load data bye or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received
C0H	Read data byte in I²C0DAT has been transmitted; NOT ACK has been received	No I²C0DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		no I²C0DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'
		no I²C0DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		no I²C0DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'. A START condition will be transmitted when the bus becomes free
C8H	Last read data byte in I²C0DAT has been transmitted (AA=0); ACK has been received	No I²C0DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		no I²C0DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'
		no I²C0DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		no I²C0DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if I²C0ADR(0) = '1'. A START condition will be transmitted when the bus becomes free

Table 130: I²C Miscellaneous status codes

Status Code I²C0STA	Status of the I²C Bus and SIO1 Hardware	Application embedded firmware Response					Next Action Taken By SIO1 Hardware
		To /from I²C0DAT	TO I²C0CON				
			STA	STO	SI	AA	
00H	Bus error	No I²C0DAT action	X	1	0	X	Hardware will enter the “not addressed” slave mode
F8H	No information available	No I²C0DAT action	--	--	--	--	--

9.11.7.4 I²C0ADR Register

The CPU can read from and write to this 8-bit SFR. I²C0ADR is not affected by the SIO1 hardware. The contents of this register are irrelevant when SIO1 is in a master mode. In the slave modes, the seven most significant bits must be loaded with the microcontroller’s own slave address, and, if the least significant bit is set, the general call address (00H) is recognized; otherwise it is ignored.

Table 131: I²C0ADR Register (SFR: address DBh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SA(6:0)							GC
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 132: Description of I²C0ADR Register bits

Bit	Symbol	Description
7 to 1	SA(6:0)	**Slave address.** These bits correspond to the 7-bit slave address which will be recognized on the incoming data stream from the I2C bus. When the slave address is detected and the interface is enabled, a serial interrupt will be generated to the CPU.
0	GC	**General call.** This bit, when set, will cause the I2C logic to watch for the general call address to be transmitted on the I2C bus. If a general call address is detected and this bit is set, a serial interrupt will be generated to the CPU.

9.12 HIGH SPEED UART

The High Speed Universal Asynchronous Receiver and Transmitter is implemented to facilitate high speed link to the host.

9.12.1 Feature list

The characteristics of the UART are the following:

- Full duplex serial port
- Receive buffered to allow reception of byte while the previous bytes are stored into the FIFO manager
- 8 bits data transfers at various baud rates
- High speed communication
- Common programmable baud rate generator using prescaler for transmission and reception
- Based on 27.12 MHz clock frequency
- preamble filter
- wake-up generator

9.12.2 High Speed UART Block Diagram

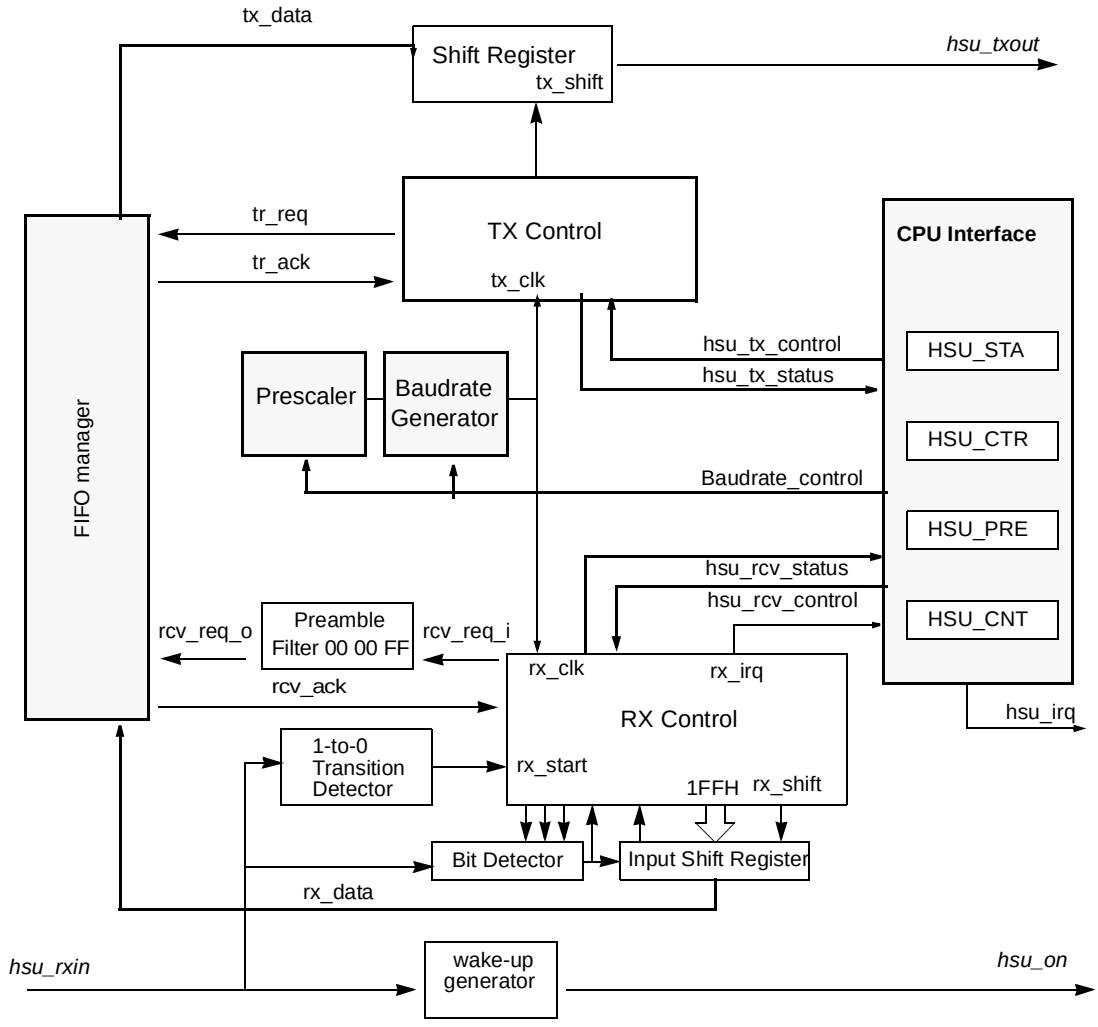


Fig 30. High Speed UART block diagram

9.12.3 High Speed UART Functional Description

The HS UART module is an Asynchronous Universal Receiver Transmitter. It is a full duplex serial port which means it can transmit and receive simultaneously. The serial port is receive-buffered: In conjunction with the FIFO manager, the reception of several bytes can be performed without too strong CPU real time constraints. However, if the received fifo still has not been read by the CPU, and the number of receive byte is greater than the receive fifo size then the new incoming bytes will be lost.

The serial port receive and transmit data registers are both accessed by embedded firmware at the address of Special Function Register of the FIFO manager. Writing to FDATA loads the transmit register, reading from SDATA accesses the separate receive register.

9.12.3.1 Mode of operation

The HS UART support only one operational mode. This mode have the following characteristics:

- Start bit:
  - The start bit detection is detecting when a 0 is asserted on the RX line.
- 8 data bits:
  - The data bit are send or received in the order LSB first.
- Stop bit:
  - During reception, the stop bits are detected when all the data bits are received and when stop bits are sampled to 1. The number of stopbits is programmable. It can be 1 or 2.
  - During Transmission, after the complete data bit transmission, some ‘1’ are transmitted. The number od stopbits is programmable. It varies from 1 to 4.

9.12.3.2 HSU Baud rate generator

To reach the high speed transfer rate, the HS UART has it own baud rate generator. The baud rate generator is composed of mainly the Prescaler and the Counter. The prescaler is located before the counter. The purpose of the prescaler is to divide the frequency of the count signal to enlarge the range of the counter (at the cost of a lower resolution). The division factor of the prescaler is equal to 2 to the power HSU_PRE[8:0], resulting in division factors ranging from 1 (20) to 256 (28). The conjonction of these 2 blocks define the bit duration and the bit sampling.

9.12.3.3 HSU preamble filter

Received characters are transmitted to the FIFO manager after having received three consecutives characters 00 00 FF. Then the following characters of the frame are transmitted and stored in the FIFO. When the frame is finished, and before a new frame arrives, embedded firmware shall write a ‘1’ in the start_frame of the HSU_CTR register to re-active the 00 00 FF filter. If embedded firmware does not write a ‘1’ then all characters of the frame are transmitted to the FIFO.

By default the preamble filter is active. It can be disabled when writing a ‘1’ in the disable_0000FF bit in the HSU_STA register. In this mode, all characters of the frame are transmitted to the FIFO.

9.12.3.4 HSU wake-up generator

The wake-up generator is a 3 bit counter which counts on every rising edge of hsu_rxin. When the counter reaches 5 the hsu_on signal is asserted in order to wake-up the system. This bloc is useful in Power-down mode. embedded firmware shall reset this counter just before going in Power down by writing a ‘1’ in the hsu_wu_en in the HSU_CTR register.

9.12.4 HSU Register Description

9.12.4.1 HSU SFR Register List

The UART contains 4 SFRs:

Table 133: High speed UART SFR Register List

Name	Size [bytes]	SFR Address	Description	Access
HSU_STA	1	ABh	High Speed UART STAtus register	R/W
HSU_CTR	1	ACh	High Speed UART ConTROl register	R/W
HSU_PRE	1	ADh	High Speed UART Prescaler for Baud rate generator	R/W
HSU_CNT	1	AEh	High Speed UART CouNTer for Baud rate generator	R/W

9.12.4.2 Register HSU_STA

The Special Function Register HSU_STA is the status register of the UART. This register contains the mode selection bits (SM2, SM1, SM0), the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 134: HSU_STA Register (SFR: address ABh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	set_bit	-	-	disable_ 0000FF	irq_rx_over _en	irq_rx_fer_ en	irq_rx_over	irq_rx_fer
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 135: Description of HSU_STA Register bits

Bit	Symbol	Description
7	set_bit	**When this bit is set to 0 during write operation, the marked bit is written to 0. When this bit is set to 1during write operation, the marked bit is written to 1.** This bit define the value to set into the other bits of this register when the other bits are set to 1.
6 to 5	-	Not used
4	disable_0000FF	**Disable the preamble filter.** When set to 1, this bit disables the preamble filtering, it means that RX line transmit any received bytes to the FIFO manager.
3	irq_rx_over_en	**Enable fifo overflow interrupt (CONTROL BIT).** When set to 1, this bit enables the interrupt generation when the bit irq_rx_over is set to 1.
2	irq_rx_fer_en	**Enable framing error interrupt (CONTROL BIT).** When set to 1, this bit enables the interrupt generation when the bit irq_rx_fer is set to 1.
1	irq_rx_over	**Receive fifo overflow interrupt.** This bit is set when the fifo manager is full (rcv_ack = ‘0’) and when the shift register is ready to transmit another byte.
0	irq_rx_fer	**Framing error interrupt.** This bit is set when a framing error has been detected. The framing error detection is only based on the stop bit sampling. When an expected stopbit bit at ‘1’ is sampled to ‘0’, this bit is asserted.

9.12.4.3 Register HSU_CTR

This register control the configuration of the high speed UART.

Table 136: HSU_CTR Register (SFR: address ACh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	hsu_wu_en	start_frame	tx_stopbit		rx_stopbit	tx_en	rx_en	soft_reset_n
Reset	X	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 137: Description of HSU_CTR Register bits

Bit	Symbol	Description
7	hsu_wu_en	**hsu wake-up enable.** When set to 1 this bit re-activates the hsu_rxin rising_edge counter. When the counter is 5 then a signal hsu_on is active. This signal is one of the wake-up reasons from Power down mode in the PCR bloc. embedded firmware shall set this bit just before requesting a power-down.
6	start_frame	**Enable the preamble filter for next frame.** When set to 1 this bit indicates that a new frame is coming. This re-activates the preamble filter (when enabled), meaning that the fist 00 00 FF characters will not be transmitted to the fifo manager, but the following ones will be.
5 to 4	tx_stopbit	**Define the number of stop bit during transmition. The number of stop bit is equal to rx_stopbit+1.** These 2 bits define the number of stop bits (a logical 1 on the hsu_tx_out line) inserted at the end of the transmission frame. The number of stop bit inserted is equal to tx_stopbit +1.
3	rx_stopbit	When set to 0 defines that the receive frame uses one stop bit. When set to 1 defines that the receive frame uses two stop bits.
2	tx_en	**Enable the transmition of the high speed UART.** When set to 1 this bit enable the transmission of characters. When this bit is set to 0, the transmission becomes disabled only after the completion of the on going transmission if any.
1	rx_en	**Enable the reception of the high speed UART.** When set to 1 this bit enables the reception of characters. When this bit is set to 0, the reception becomes disabled only after the completion of the on going transmission if any.
0	soft_reset_n	**Active low embedded firmware Reset .** When set to ‘0’ this bit disable the clock of the RX control, TX control and BAUd rate generator modules.

9.12.4.4 Register HSU_PRE

This register is used to configure the prescaler.The prescaler enlarge the range of the counter (at the cost of a lower resolution). The division factor of the prescaler is in division factors ranging from 1 (20) to 256 (28).

Table 138: HSU_PRE Register (SFR: address ADh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	hsu_prescaler							
Reset	18	18	18	18	18	18	18	18
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 139: Description of HSU_PRE Register bits

Bit	Symbol	Description
7 to 0	hsu_prescaler	This byte define the high speed UART clock (CPU clock) division factor

9.12.4.5 Register HSU_CNT

This register is used to configure the counter for the baudrate generator.

Table 140: HSU_CNT Register (SFR: address AEh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	hsu_counter							
Reset	70	70	70	70	70	70	70	70
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 141: Description of HSU_CNT Register bits

Bit	Symbol	Description
7 to 0	hsu_counter	This byte is used in conjunction to define the baud rate.Baudrate= fclk / ((hsu_prescaler +1) * hsu_counter)

9.13 USB

The USB module is an USB2.0 compliant device with embedded function.
Special power management features such as a clock divider and clock switch are also implemented in the device.

9.13.1 Features list

The USB module is a USB device only supporting full speed communication scheme. All embedded functions are passed to the microcontroller.

The USB module includes the following features:

- SoftConnect supported
- Command GetFrameNumber supported
- Interrupt signaling to microcontroller
- Control EP0 endpoint of 8 bytes
- 3 interrupt endpoints of 8 bytes
- 2 bidirectional bulk endpoints of 64 bytes
- resume by host
- remote wake-up

The endpoints setup is described in the following table.

Table 142: Endpoints Setup

Logical Endpoints	OUT Type	IN Type	OUT Map	IN Map	OUT size	IN size	Note
Device Function Description							
0	Control	Control	0.0	0.1	8	8	
1	-	Int	-	0.2		8	
2	-	Int	-	0.3		8	
3	-	Int	-	0.4		8	
4	Bulk	Bulk	0.5	0.6	64	64	

9.13.2 USB interrupt

The interrupt line of the USB module is asserted to indicates to the microcontroller that there was a transaction on one of the endpoints, or that there is new status information available.

9.13.3 Resume by host

9.13.3.1 Resume by host in suspend state

After 3 ms of no USB activity on the bus, the device goes in suspend. About 2 ms later the device will indicate that it no longer needs the clock (Clk_Enable_N becomes inactive).

The host can then send a resume to the device. The device needs to wake-up and will require the main clock (USB_Clk_Enable_N becomes active). The main clock starts running after complete PCR wake-up sequence. PLL_LOCK indicates that the main clock is running stable (a PLL can need several µs to start running at the specified frequency). The device then knows that the clock is present and can go out of suspend.

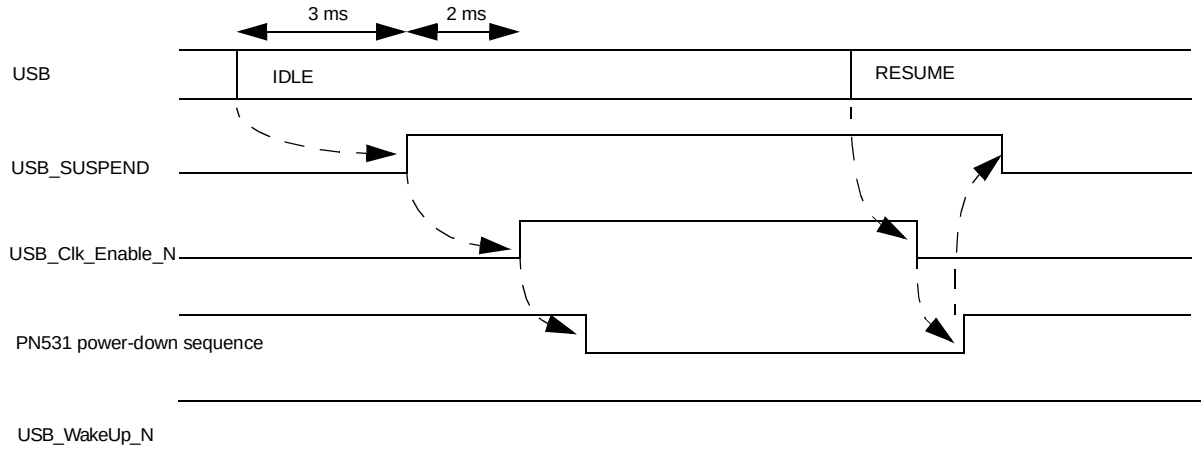


Fig 31. Resume by host / clocks stopped

9.13.3.2 Resume by Host before clock is disabled

The host can decide to wake-up a suspended device, before the device has switched off its main clock. The device then simply goes out of suspend.

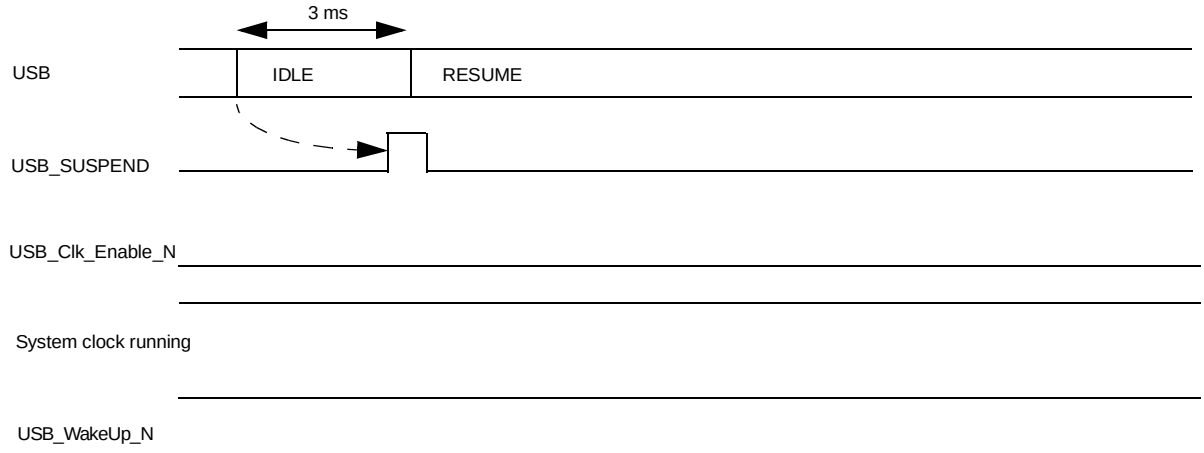


Fig 32. Resume by host / clocks running

9.13.4 Remote wake-up

The remote wake-up implemented in the PN531 platform is partly controlled by the microcontroller as depicted below:

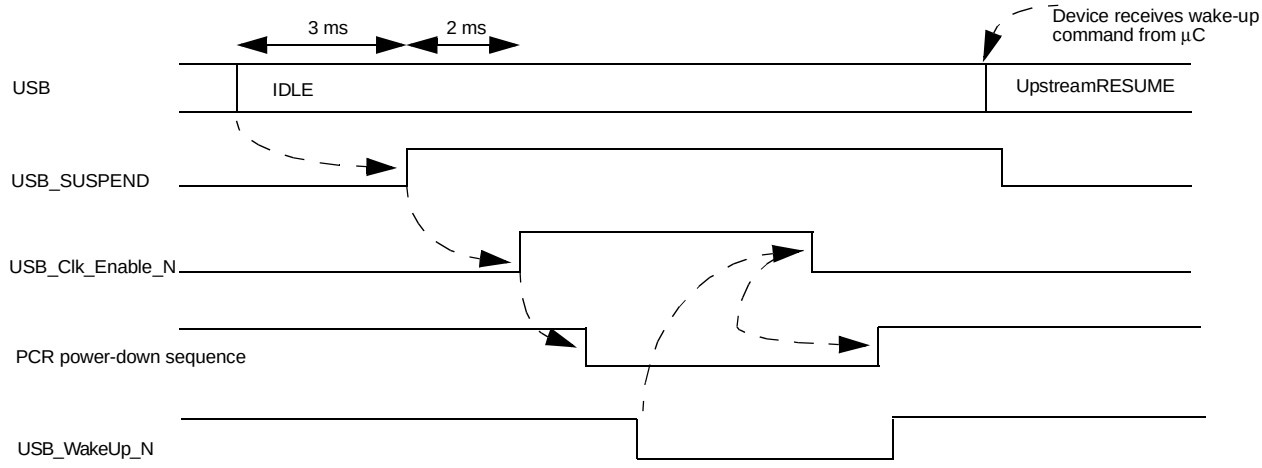


Fig 33. RemoteWakeUp by µC

When a remote wake-up is requested on an external interrupt (P32_INT0, P33_INT1) or a RF detector event, the Power Clock and Reset controller (PCR):

- enables the 27.12 MHz oscillator
- generates an interrupt to resume the CPU from Power-down mode
- then the CPU enable the 4 MHz oscillator, the PLL and the 48 MHz clock.

The CPU sends a command to the USB module to perform a USB remote wake-up, then the USB module exits from suspend mode and sends a resume on its upstream port.

9.13.4.1 Resume by Remote Wake-up before clock is disabled

Resume by Remote Wake-up before clock is disabled

If USB_WakeUp_N is made active before the main clock is switched off (USB_Clk_Enable_N becomes inactive), the device waits until it has been suspended for 2 ms, then wakes up and sends a resume on its upstream port.

9.13.5 Softconnect

The following figure shows how the embedded firmware Controlled Connect can be implemented.

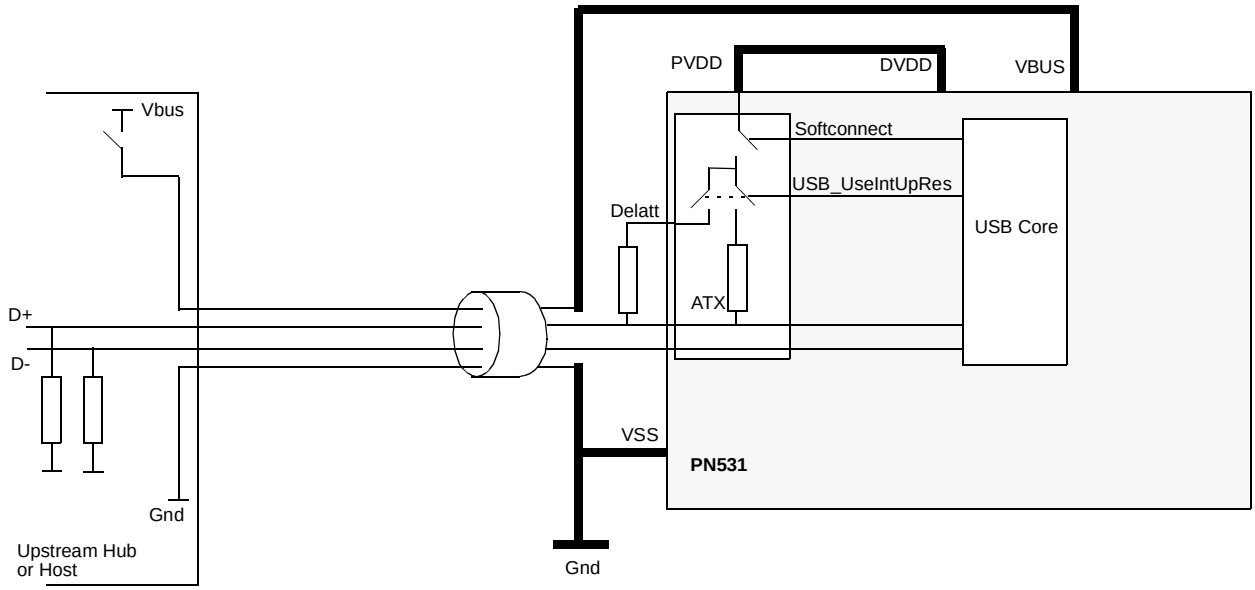


Fig 34. SoftConnect Connection

When USB_SoftConnect_N is active, one of the data lines (D+) must be pulled high. This is done by using internal switch.

The internal pull up resistor or an external resistor (connected to delatt) can be used to perform the soft connection. The selection of the pull-up resistor to use is made through the USB configuration register. Refer to Table 142 “USB configuration Register (6000h)” on page 103.

9.13.6 USB embedded firmware View

The USB module is mapped into the XRAM memory space. It is accessible into the peripheral area on the host if internal bus. The communication between the CPU and the USB module is based on a sequence of command and data exchange.

Table 143: USB Extension memory map

Physical Address		Size (bytes)	Description	Peripheral selected
First	Last			
6003h	6003h	1	Write command to USB module	USB
6002h	6002h	1	Write data to USB module	USB
6001h	6001h	1	Read data from USB	USB
6000h	6000h	1	USB configuration	USB

Table 144: USB configuration Register (address 6000h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	USB_UseIntUpRes	-	-	-	-	-
Reset	X	X	0	X	X	X	X	X
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

Table 145: Description of USB configuration Register bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5	USB_UseIntUpRes	It controls switch for internal Upstream resistor.
4 to 0	-	Reserved.

9.13.6.1 USB Instruction set

The USB instruction set is described here after.

Table 146: USB Instruction set

Name	Recipient	Coding	Data Phase
Get Chip ID	Device	FDh	Read 2 bytes
Get ErrorCode	Device	FFh	Read 1 byte
Get Device Status	Device	FEh	Read 1 byte
Set Device Status	Device	FEh	Write 1 byte
Get Current Frame Number	Device	F5h	Read 2 bytes
Get Interrupt Register	Device	F4h	Read 2 bytes
Set Mode	Device	F3h	Write 2 bytes
Set Endpoints Enable	Device	D8h	Write 2 bytes
Set Address / Enable	Embedded Function	D0h	Write 1 byte
Select Endpoint	Function Control OUT	00h	Read 1 byte (opt)
	Function Control IN	01h	Read 1 byte (opt)
	Function Endpoint 1 IN	02h	Read 1 byte (opt)
	Function Endpoint 2 IN	03h	Read 1 byte (opt)
	Function Endpoint 3 OUT	04h	Read 1 byte (opt)
	Function Endpoint 3 IN	05h	Read 1 byte (opt)
	Function Endpoint 4 IN	06h	Read 1 byte (opt)
	Reserved	07h	-
	Reserved	08h	-
	Reserved	09h	-
Select Endpoint / Clear Interrupt	Function Control OUT	40h	Read 1 byte
	Function Control IN	41h	Read 1 byte
	Function Endpoint 1 IN	42h	Read 1 byte
	Function Endpoint 2 IN	43h	Read 1 byte
	Function Endpoint 3 OUT	44h	Read 1 byte

Table 146: USB Instruction set

Name	Recipient	Coding	Data Phase
	Function Endpoint 3 IN	45h	Read 1 byte
	Function Endpoint 4 IN	46h	Read 1 byte
	Reserved	47h	-
	Reserved	48h	-
	Reserved	49h	-
Set Endpoint Status	Function Control OUT	40h	Write 1 byte
	Function Control IN	41h	Write 1 byte
	Function Endpoint 1 IN	42h	Write 1 byte
	Function Endpoint 2 IN	43h	Write 1 byte
	Function Endpoint 3 OUT	44h	Write 1 byte
	Function Endpoint 3 IN	45h	Write 1 byte
	Function Endpoint 4 IN	46h	Write 1 byte
	Reserved	47h	-
	Reserved	48h	-
	Reserved	49h	-
Read Buffer	Selected Endpoint	F0h	Read n bytes
Write Buffer	Selected Endpoint	F0h	Write n bytes
Clear Buffer	Selected Endpoint	F2h	Read 1 byte (opt)
Validate Buffer	Selected Endpoint	FAh	none

9.13.6.2 Get VChip ID

Command: FDh

Data: Read 2 bytes

The Chip Identification is 12 bits wide. The command divides the chip Identification in bytes and returns the least significant byte first. The value of this chip ID can be determined at integration time.

The following table shown the configuration of these 2 bytes:

Table 147: Get Chip ID bytes

Bit Position	7	6	5	4	3	2	1	0
Byte 0	DEVREV[1]							
Byte 1	0	0	0	0	DEVNAME[2]			

[1] hardware setting (8 bits) same as DEVREV, see “Device Descriptor”.

2] hardware setting (4 bits) same as DEVNAME, see “String Descriptor”

9.13.6.3 Get ErrorCode

Command: FFh

Data: Read 1 byte

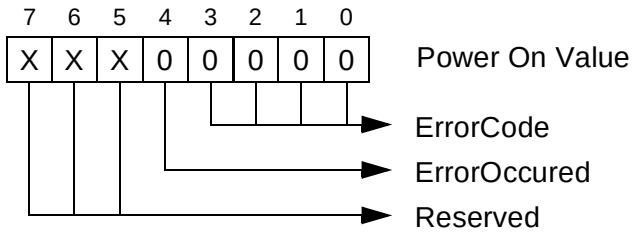


Fig 35. ErrorCode Register

Note that this is a debug command and should not be used for normal operation.

The 'Get Error Code command returns the error code of the last generated error, this command is for debugging purposes only. The 4 least significant bits form the error code. Bit 4 'Error Occurred' can be cleared by each new transfer

The following table gives an overview of the Error Codes.

Table 148: Error codes

Error Code	Description
0000	No Error
0001	PID Encoding Error
0010	Unknown PID
0011	Unexpected Packet
0100	Error in Token CRC
0101	Error in Data CRC
0110	Time Out Error
0111	Babble
1000	Error in End of Packet
1001	Sent NAK
1010	Sent Stall
1011	Buffer Overrun Error
1100	Sent Empty Packet (ISO only)
1101	Bitstuff Error
1110	Error in Sync
1111	Wrong Toggle Bit in Data PID, ignored data

9.13.6.4 Get Device Status

Command: FEh

Data: Read 1 byte

The Get Device Status command returns the Device Status Register. Cf. the Set Device Status command.

When SuspendChange, ConnectChange and BusReset bit are set, the appropriate bit in the interrupt register is set and an interrupt is generated to the microcontroller.

The BusReset, SuspendChange and ConnectChange bit are reset by this command.

9.13.6.5 Set Device Status

The Set Device Status command changes the Device Status Register. The value of Read Only bits is ignored.

Table 149: Device Status Register (address FEh) bit allocation; Data: Write 1 byte

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	Reset	SuspendChange	Suspended	ConnectChange	Connect
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R	R	R/W	R	R/W

Table 150: Description of HSU_CTR Register bits

Bit	Symbol	Description
7 to 5	-	Reserved.
4	Reset	**The Reset bit is set when the device receives a bus reset.** It is cleared when read.On a bus reset the device will automatically go to the default state (unconfigured and responding to address 0).
3	SuspendChange	**The Suspend Change bit is set to '1' when the Suspend bit toggles.** The Suspend bit can toggle because: • The device goes in the suspendedstate • The device receives resume signallingon its upstream portThe Suspend Change bit is reset after the register has been read.
2	Suspended	**The Suspend bit represents the current Suspend state.** It is set to '1' when the device hasn't seen any activity on its upstream port for more than 3 ms. It is reset to '0' on any activity.When the device is suspended (Suspend bit = '1') and the microcontroller writes a '0' into it, the device will generate a remote wake-up. When the device is not suspended, writing a '0' has no effect. Writing a '1' into this register has never an effect.
1	ConnectChange	**Change of the connect status.** Reading clears the bit.
0	Connect	**Writing '1' will allow the device to connect its pull up resistor.** Writing '0' forces a disconnect. Reading returns the current connect status.

9.13.6.6 Get Current Frame Number

Command: F5h

Data: Read 1 or 2 byte(s)

Data: Write 2 bytes

9.13.6.7 Configuration byte

Table 151: Configuration byte Register (address F5h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	RemoteWakeUp Enable	AlwaysPLLClock	-	-	Interrupt OnNAK
Reset	X	0	0	0	0	0	X	1
Access								

Table 152: Description of Configuration byte Register bits

Bit	Symbol	Description
7 to 5	-	Reserved.
4	RemoteWakeUpEnable	**A '1' indicates that the remote wake-up feature is enabled.** The upstream remote wake up can be activated by through the RemoteWakeUp_N pin of USB module when the device is suspended.
3	AlwaysPLLClock	**A '1' indicates that the internal clocks and PLL are always running even during suspend state.** A '0' indicates that the internal clock, crystal oscillator and PLL are stopped whenever not needed. To meet the strict suspend current requirement, this bit needs to be set to '0'.
2 to 1	-	Reserved.
0	InterruptOnNAK	**A '1' indicates that "NAKing" is reported and will generate interrupt.** A '0' indicates that only successful transactions are reported.

9.13.6.8 Clock division

Table 153: Clock division Register (address xxh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	ClkDivFactor					
Reset	X	X	0	0	0	0	1	1
Access								

Table 154: Description of Clock division Register bits

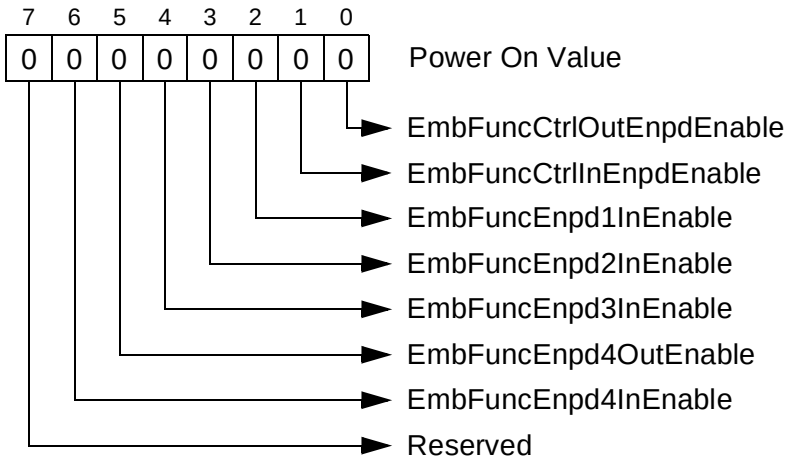
Bit	Symbol	Description
7 to 6	-	Reserved. Write 0.
5 to 0	ClkDivFactor	**The value indicates clock division factor for CLOCKOUT.** The output frequency is 48 MHZ/(N+1) where N is the Clock Division Factor. The reset value is 3. This will produce the output frequency of 12 MHZ which can then be programmed up (or down) by the user. This design ensures no glitching during frequency change. The programmed value will not be changed by a bus reset.

9.13.6.9 Set Endpoints Enable

Command: D8h

Data: Write 2 bytes

Byte 1:



Byte 2:

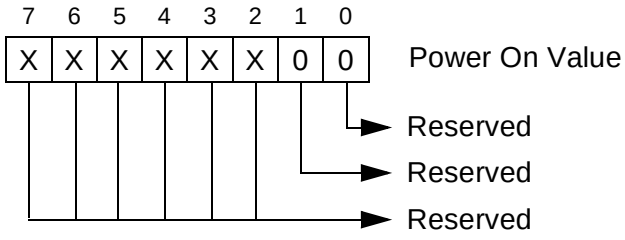


Fig 36. Endpoints Enable bytes

This command provides endpoint enable. The enable is defined on physical endpoint level meaning that for one endpoint the IN and OUT direction can be enabled separately.

9.13.6.10 Set Address / Enable

Table 155: Address/Enable byte Register (address D0h) bit allocation; Data: Write 1 byte

Bit	7	6	5	4	3	2	1	0
Symbol	DevEnable	DevAddress						
Reset	X	0	0	0	0	0	0	0
Access								

Table 156: Description of Address/Enable byte Register bits

Bit	Symbol	Description
7	DevEnable	A ‘1’ enables this function
6 to 0	DevAddress	The value written becomes the address.

9.13.6.11 Select Endpoint

This command initializes an internal pointer to the start of the Selected buffer. Optionally, this command can be followed by a data read, which returns some additional info on the packet in the buffer.

Table 157: Select Endpoint Byte Register (address 00h - 09h) bit allocation; Read 1 byte (Optional)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	SentNAK	PacketOverwritten	SetupPacket	StallStatus	FullEmptyStatus
Reset	X	X	X	0	0	0	0	0
Access								

Table 158: Description of Select Endpoint Byte Register bits

Bit	Symbol	Description
7 to 5	-	Reserved.
4	SentNAK	**’1’: The device has sent a NAK.** If the host sends an OUT packet to a filled OUT buffer, the device returns NAK. It the host sends an IN token to an empty IN buffer, the device returns NAK.This bit is set when a NAK is sent and the Interrupt On NAK feature is enabled. This bit is reset after the device has sent an ACK after an OUT packet or when the device has seen an ACK after sending an IN packet. This bit is only defined for the two physical control endpoints.
3	PacketOverwritten	’**1’: The previously received packet was over written by a setup packet.** The value of this bit is cleared by the ’Select Endpoint/Clear Interrupt’ command.
2	SetupPacket	**A "1" indicates the last received packet for the selected endpoint was a setup packet.** The value of this bit is updated after each successfully received packet (i.e. anACKED package on that particular physical endpoint).It is cleared by doing a Select Endpoint/Clear Interrupt on this endpoint
1	StallStatus	**A "1" indicates the selected endpoint is in the stall state.**
0	FullEmptyStatus	**A "1" indicates the buffer of the selected endpoint is full, "0" indicates an empty buffer.** In case of an OUT endpoint, this bit is cleared by executing the Clear Buffer Command, if the buffer has not been over written.In case of an IN endpoint, this bit is set by the Validate Buffer command.

9.13.6.12 Select Endpoint / Clear Interrupt

Command: 40h - 49h

Data: Read 1 byte

Commands 40h to 49h are identical to their Select Endpoint equivalent, with the following differences:

- The command clears the associated interrupt
- The command clear the Setup and Overwritten bits in case of a control out endpoint
- The read of one byte is mandatory

9.13.6.13 Set Endpoint Status

Table 159: Endpoint Status byte Register (address 40h - 49h) bit allocation; Write 1 byte

Bit	7	6	5	4	3	2	1	0
Symbol	Conditional Stall	RateFeedback Mode	Disable	-	-	-	-	Stalled
Reset	0	0	0	X	X	X	X	0
Access								

Table 160: Description of Select Endpoint Byte Register bits

Bit	Symbol	Description
7	Conditional Stall	’1’: Stall both endpoint zero endpoints, unless the ’Setup Packet’ bit is set. It is only defined for control OUT endpoints
6	RateFeedbackMode	’0’: Interrupt endpoint in ’toggle mode’ ’1’: Interrupt endpoint in ’rate feedback mode’
5	Disable	A “1” indicates the endpoint is disabled. After a bus-reset each endpoint is enabled, i.e., this bit is set to ’0’.
4 to 1	-	Reserved.
0	Stalled	A “1” indicates the endpoint is stalled.

9.13.6.14 Read Buffer

Command: F0h

Data: Read up to n+2 bytes

'n' is equal to the number of data bytes in the selected buffer.

This command is followed by a number of data reads, which return the contents of the selected endpoint data buffer. After each read, the internal buffer pointer is incremented by 1.

The buffer pointer is not reset to the beginning of the buffer by this command. This means that reading or writing a buffer can be interrupted by any other command (except for Select Endpoint).

The data in the buffer are organized as follow:

Table 161: Read Buffer bytes

Bit Position	7	6	5	4	3	2	1	0
Byte 0	0/1	0/1	-	-	-	-	-	-
Byte 1	-	Number of Data bytes in buffer						
Byte 2	Data byte 0							
...								
Byte n+1	Data byte n -1							

9.13.6.15 Write Buffer

Command: F0h

Data: Write up to n+2 bytes

'n' is equal to the number of data bytes in the selected buffer.

This command is followed by a number of data writes, which load the data buffer of the selected endpoint. After each write, the internal pointer is incremented by 1. The buffer pointer is not reset to the beginning of the buffer by the Write Buffer command. This means that writing a buffer can be interrupted by any other command (except for Select Endpoint).

The data in the buffer are organized as follow:

Table 162: Write Buffer bytes

Bit Position	7	6	5	4	3	2	1	0
Byte 0	0/1	0/1	-	-	-	-	-	-
Byte 1	-	Number of Data bytes in buffer						
Byte 2	Data byte 0							
...								
Byte n+1	Data byte n -1							

9.13.6.16 Clear Buffer

Command: F2h

Data: Read 1 byte (Optional)

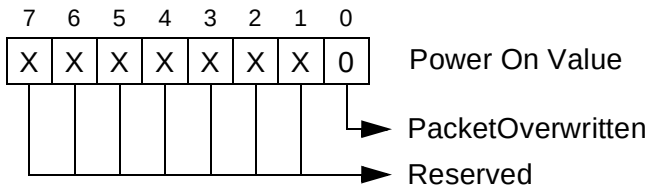


Fig 37. Clear Buffer byte

When a packet is received completely, an internal endpoint buffer full flag is set. All subsequent packets will be refused by returning a NAK. When the microcontroller has read the data, it should free the buffer by the Clear Buffer command. When the buffer is cleared new packets will be accepted.

When bit '0' of the optional data byte is '1', the previously received packet was over written by a Setup Packet. A buffer cannot be cleared when its Packet Overwritten bit is set.

9.13.6.17 Validate Buffer

Command: FAh

Data: None

When the microprocessor has written data into an IN buffer, it should set the buffer full flag by the Validate Buffer command.

This indicates that the data in the buffer is valid and can be sent to the host when the next IN token is received. A control IN buffer cannot be validated when the Packet Overwritten bit of its corresponding OUT buffer is set.

9.14 SPI

9.14.1 Feature list

- Compliant with Motorola Serial Peripheral Interface (SPI) specification
- Synchronous, Serial, Half-Duplex communication, 5 MHz max
- Slave configuration
- 8 bits bus interface

The HOST through the SPI interface can either access to the fifo (acting as data buffer) or a status register. This selection can be made through the protocol supported during the communication.

9.14.2 SPI structure

9.14.2.1 Pointer for the shift register

A shift register is used to address the SPI interface. The value loaded in this register is either the first byte of the FIFO or the status register's content.

It depends on the first byte received from the host. The first character sent by the host will content the register to address (STATUS or DATA) and also if it is a write or a read operation. This character will be managed by hardware.

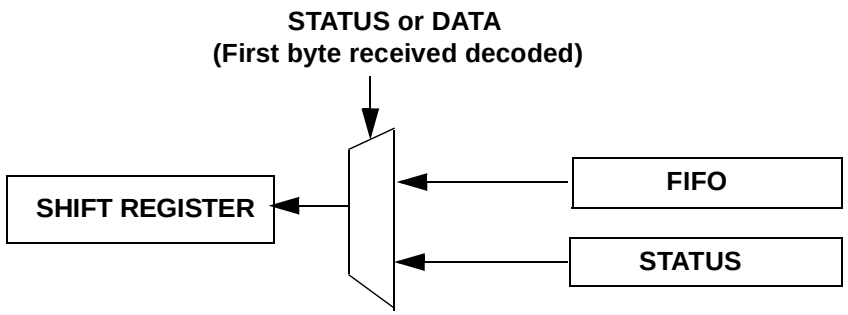


Fig 38. Memory manager shift register management

9.14.3 Protocol

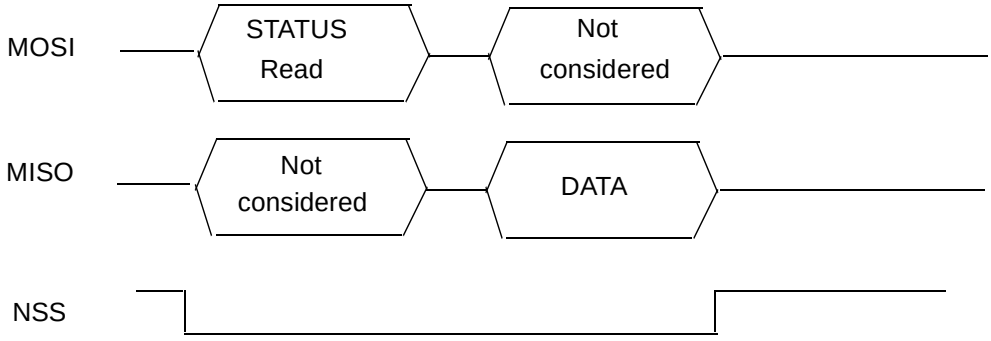
The SPI data exchange between the PN531 and the Host is based on the light protocol. Once the FIFO is full enough, the CPU set the bit ready in the status register. The host polling the status register is informed of the ready flag. Once this bit is set, the host can start the data transfer.

The protocol used is based on:

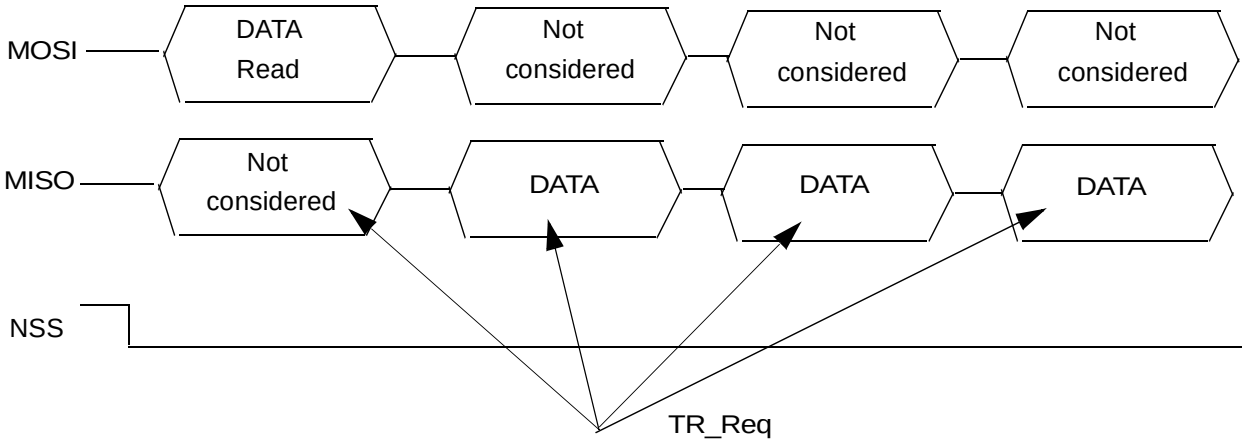
- An ADRESS / DATA protocol for status data exchanges
- An ADRESS / DATA / DATA / DATA ... for a data transfer (FIFO)

An exchange starts on the falling edge of NSS and follow the diagram describes here after.

STATUS read access:



FIFO read access



FIFO write access

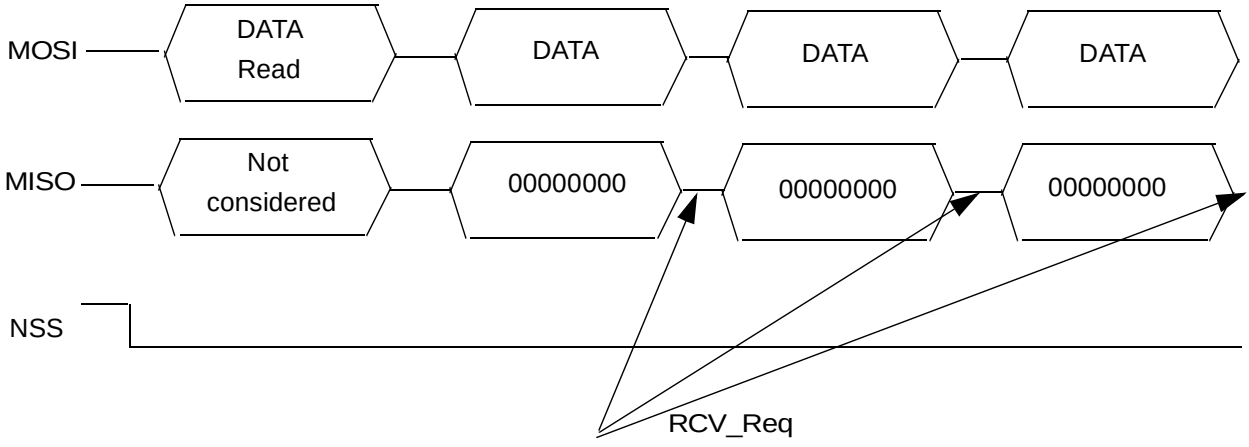


Fig 39. Protocol data management.

9.14.3.1 First character

It contains the address on which the pointer of the shift register is going to be linked. It also defines if this register will be accessed for a read or a write operation.The decoding of this first character is done by hardware.

The bits needed to define the following operations are the first bit of the first byte.

Table 163: SPI operation opcode

Bit 1	Bit 0	Operation
0	1	data reception
1	0	status transmission
1	1	data transmission

9.14.3.2 Following characters for READ STATUS register

Their is in that case no read request going to the FIFO manager.
The content of the status register is loaded in the shift register.
The character received on MOSI is not considered.

9.14.3.3 Following characters for READ DATA Buffer

A character is loaded from the FIFO into the SPI shift register.
The character received on MOSI is not considered. The character received on MOSI is not considered.

9.14.3.4 Following characters for WRITE DATA Buffer

Their is no read request generated to the fifo manager. The value “00000000” is loaded in the shift register and transmitted on MISO.
Once a character is received, a write request is sent to the FIFO manager and the character is loaded from the shift register into the reception part of the FIFO.

9.14.4 SPI SFR Register List

2 registers are needed to manage the SPI interface. These 2 registers are done with SFR.

Table 164: SPI SFR Register List

Name	Size [bytes]	SFR Address	Description	R/W
Region 1				
Control	1	A9h	Global control	R/W
Status	1	AAh	Global Status/Error messages	R

9.14.4.1 Control Register

The SPI control register is byte addressable.It contains a number of programmable bits used to control the function of the SPI block. The settings for this register must be set up prior to a given data transfer taking place.

Table 165: SPI Control Register (SFR: address A9h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	Enable	-	CPHA	CPOL	IE1	IE0
Reset	X	0	X	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 166: Description of SPI Control Register bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use. Set to 0 .
5	Enable	**Enable:** If set to 1, this bit enables the use of the SPI interface; otherwise it disables it.
4	-	Reserved for future use. Set to 0 .
3	CPHA	**Clock PHAse:** This bit controls the relation ship between the data and the clock on SPI transfers. 0: Data is always sampled on the first clock edge of SCK. 1: Data is always sampled on the second clock edge of SCK.
2	CPOL	**Clock POLarity:** This bit controls the polarity of SCK clock. If set to 1, SCK is active low else active high
1	IE1	**Interrupt Enable 1:** This bit controls the generation of a hardware interrupt generated by TR_FE. If set to 1, the interrupt is enabled else inhibited.
0	IE0	**Interrupt Enable 0:** This bit controls the generation of a hardware interrupt generated by RCV_OVR. If set to 1, the interrupt is enabled else inhibited.

Remark: The following figure explains how can be used bits CPOLand CPHA.

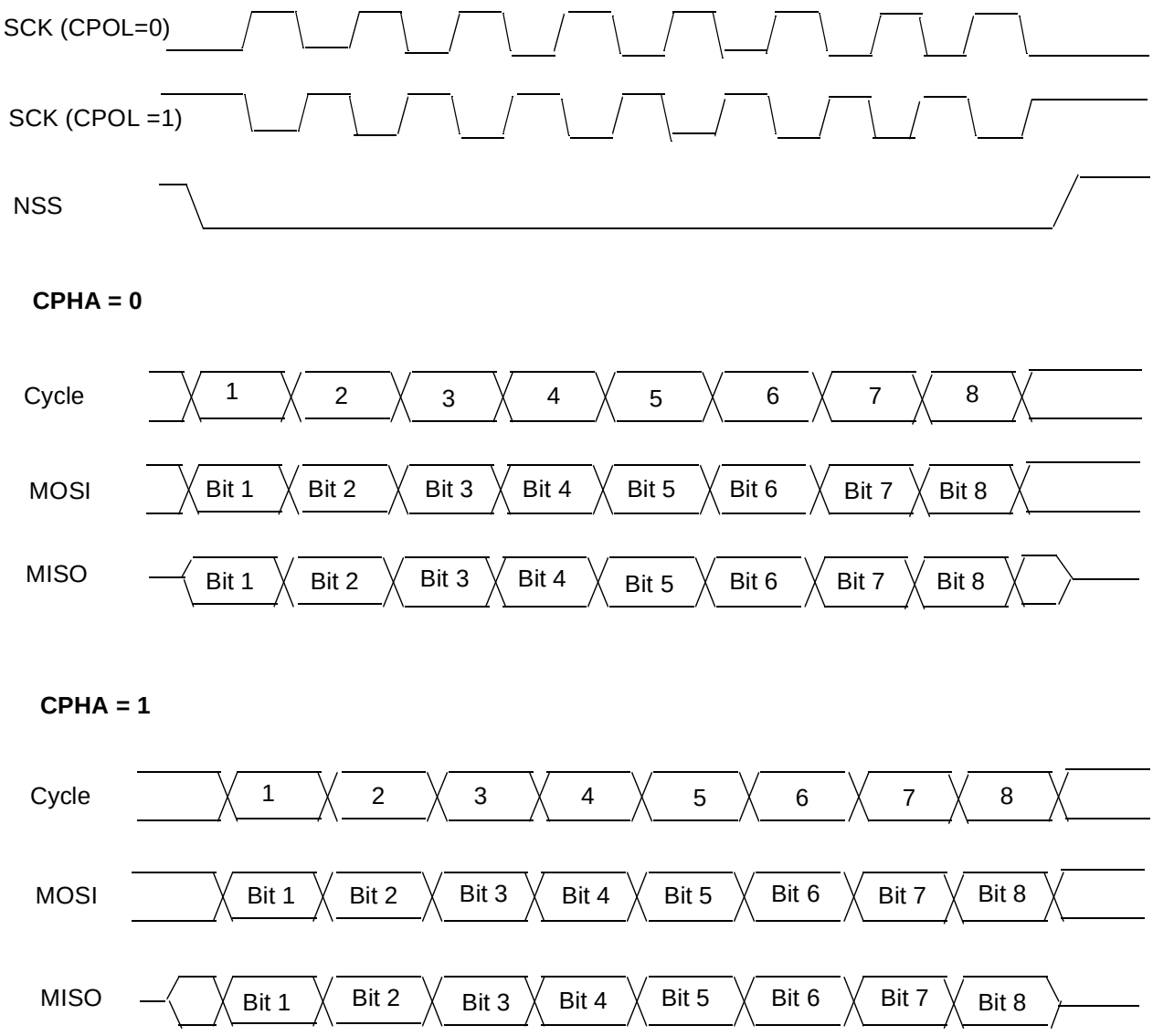


Fig 40. SPI Data transfer format

9.14.4.2 Status Register

The SPI control register is byte addressable. It contains bits which are used to monitor the status of the SPI interface, including normal functions, and exception conditions. The primary purpose of this register is to detect completion of a data transfer. The remaining bits in this register are exception condition indicators.

Table 167: SPI Status Register (SFR: address AAh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	TR_FE	RCV_OVR	WAKE-UP	READY
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

Table 168: Description of SPI Status Register bits

Bit	Symbol	Description
7 to 4	-	Reserved for future use. Set to 0.
3	TR_FE	**Transmit FIFO Empty:** This signal is set if a new character is asked to be sent and the FIFO is empty. It is reset by writing 0. This bit causes an interrupt.
2	RCV_OVR	**Receive Overrun:** This bit is set if a character is received whilst the one before has not been managed by the FIFO manager. It is reset by writing 0. This bit causes an interrupt.
1	WAKE-UP	**This bit is written by the CPU to indicate that a new commutation can start, the chip is waken-up**. This bit will be polled by the host.
0	READY	**This bit is written by the CPU to indicate that a new commutation can start.** This bit will be polled by the host.

9.15 ContactLess UART

The contact less UART manage the communication protocol according to ISO/IEC 14443-A, FeliCa and NFCIP-1. This transmission module utilises an outstanding modulation and demodulation concept completely integrated for different kinds of passive or active contactless communication methods and protocols at 13.56 MHz.

The CL UART support 3 different operating modes:

- Reader/writer mode supporting ISO/IEC 14443A/MIFARE® and FeliCa scheme.
- Card receiving mode supporting ISO/IEC 14443A/MIFARE® and FeliCa scheme.
- NFCIP-1 mode

Enabled in reader/ writer mode the CL UART internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A /MIFARE® or FeliCa cards and transponders without additional active circuitry.

The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443A compatible cards and transponders. The digital part handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The CL UART supports MIFARE® Classic (e.g. MIFARE® Standard) products. The CL UART supports contactless communication using MIFARE® Higher Baudrates up to 424 KBaud in both directions.

In the reader/ writer mode the PN531 transmission module supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection like CRC. The PN531 supports contactless communication using FeliCa Higher Baudrates up to 424 KBaud in both directions.

Enabled in card mode the PN531 transmission module is able to answer to a reader/writer command either in FeliCa or ISO/IEC 14443 A / MIFARE® card mode. The PN531generates the digital load-modulated signals and in addition with an external circuit the answers can be send back to the reader/writer.

Additionally the PN531transmission module offers the possibility to communicate directly to a second Contactless module in the NFCIP-1 mode. The NFCIP-1 mode offers different communication baudrates up to 424 KBaud. The digital part handles the complete NFCIP-1 framing and error detection.

Baudrates above 424 KBaud are supported by the digital part of the PN531module, the transmission and the reception of the high speed NFCIP-1 communication has to be done by an external circuit.

9.15.1 Feature list

- Close communication link to the analog circuitry to demodulate and decode card's response
- SFR register map for high frequency register access (16 Registers).
- Typical MOVX access to non critical registers.
- Integrated card mode detector
- Adjustable parameters to optimize the reception according to the antenna configuration
- Adjustable parameters to optimize the transmission according to the antenna configuration and characteristics.
- Supports ISO/IEC 14443A
- Supports MIFARE® Classic encryption and MIFARE® higher baudrate communication up to 424 KBaud
- Supports contactless communication according to the FeliCa scheme at 212 KBaud and 424 KBaud
- Integrated RF interface for NFCIP-1 (Near field communication) up to 424 KBaud
- Possibility to communicate in NFCIP-1 mode above 424 KBaud using external analog circuitry
- 2 interrupt sources

9.15.2 CL UART Reader/Writer Operating Mode

The modes support different transfer speeds and modulation schemes. The following chapters will explain the different modes more in detail.

Note: All indicated modulation indexes and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieved optimal performance

The CL UART support the following operating modes:

- Reader/writer mode supporting ISO/IEC 14443A / MIFARE® and FeliCa scheme.
- Card receiving mode supporting ISO/IEC 14443A / MIFARE® and FeliCa scheme.
- NFCIP-1 mode

9.15.2.1 Reader/Writer mode

Generally 2 reader/writer-operating modes are supported. The PN531 can act as a reader / writer for ISO/IEC 14443A or FeliCa cards.

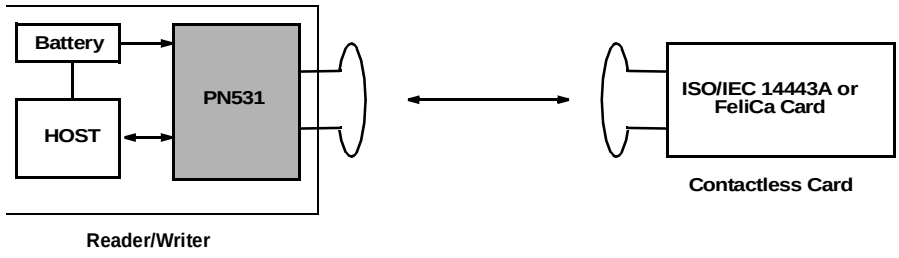


Fig 41. Reader/Writer Mode

In the reader/writer mode the Contact less UART enables the communication to a contacless ISO/IEC 14443A/MIFARE® or FeliCa card.

9.15.2.2 ISO/IEC 14443A Reader/Writer Functionality

The ISO/IEC 14443A/MIFARE® reader/writer mode is the general reader to card communication scheme according to the ISO/IEC 14443A/MIFARE® specification. The following diagram describes the communication on a physical level, the communication table describes the physical parameters (see Table 169).

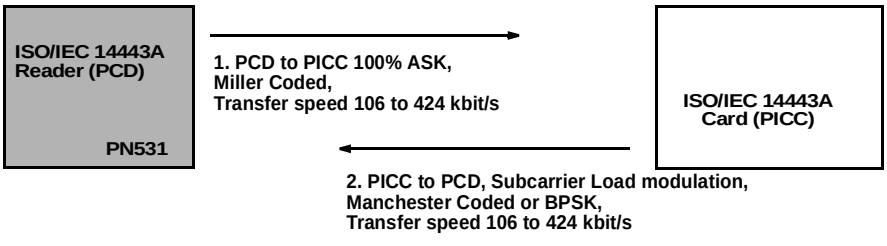


Fig 42. ISO/IEC 14443A / MIFARE® reader/writer communication diagram

Table 169: Communication overview for ISO/IEC 14443A / MIFARE® reader/writer

Communication direction		MIFARE® / ISO/IEC 14443A	MIFARE® Higher Baudrates	
	Baudrate	**106 KBaud**	**212 KBaud**	**424 KBaud**
PCD → PICC (send data from the PN531 to a card)	Modulation on reader side	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
	Bitlength	9.44 µs	9.44 µs / 2	9.44 µs / 4
PICC → PCD (receive data from a card)	Modulation on card side	Subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	Subcarrier frequency	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16
	bit coding	Manchester coding	BPSK	BPSK

The contactless UART the internal microcontroller of PN531and the external host handle the complete MIFARE® / ISO/IEC 14443 A protocol.

The internal CRC co-processor calculates the CRC value according to the definitions given in the ISO/IEC 14443A part 3.

9.15.2.3 FeliCa Reader/Writer Functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The following diagram describes the communication on a physical level, the communication table describes the physical parameters more detailed.

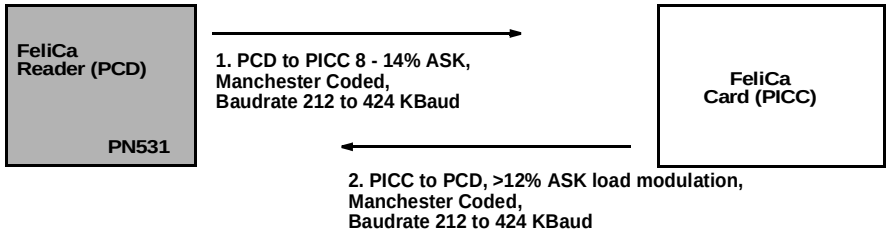


Fig 43. FeliCa communication Diagram

Table 170: Communication Overview for FeliCa reader/writer functionality

Communication direction		FeliCa	FeliCa Higher Baudrate
	Baudrate	**212 KBaud**	**424 KBaud**
PCD ->PICC (send data from the PN531to a card)	Modulation on reader side	8 - 14% ASK	8 - 14% ASK
	bit coding	Manchester coding	Manchester coding
	Bitlength	9.44 µs / 2	9.44 µs / 4
PICC->PCD (receive data from a card)	Modulation on card side	>12% ASK	>12% ASK
	bit coding	Manchester coding	Manchester coding

9.15.2.4 FeliCa Framing and Coding

Table 171: FeliCa Framing and Coding

Preamble						Sync		Len	n-Data				CRC	
00	00	00	00	00	00	B2	4D							

To enable the FeliCa communication a 6 bytes long preamble and 2 bytes Sync bytes are sent in order to synchronize the internal receiver. The Len byte is an indicator for the length of the sent data bytes plus the n-data bytes. The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF-interface the host has to send the Preamble-, Syn-, Len- and data- bytes to the PN531. Only the internal CRC calculation is added internally of the PN531.

Note: To allow a convenient detection of a FeliCa signal during data reception the 2 Sync bytes are configurable stored in one register.

Start Value for the CRC Polynomial: 00h

Table 172: FeliCa Framing and Coding

Preamble						Sync		Len	2 Data bytes		CRC	
00	00	00	00	00	00	B2	4D	03	AB	CD	90	35

9.15.3 NFCIP-1 MODE

The NFCIP-1 communication differentiates between an active and a passive communication mode.

- Active Communication Mode means both the initiator and the target are using their own RF field to transmit data
- Passive Communication Mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: generates RF field @ 13.56 MHz and starts the NFCIP
- Target: responds to initiator command either in a load modulation scheme for passive communication mode or using a self generated and self modulated RF field for active communication mode.

In order to fully support the NFCIP-1 standard the PN532 supports the active and passive communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard

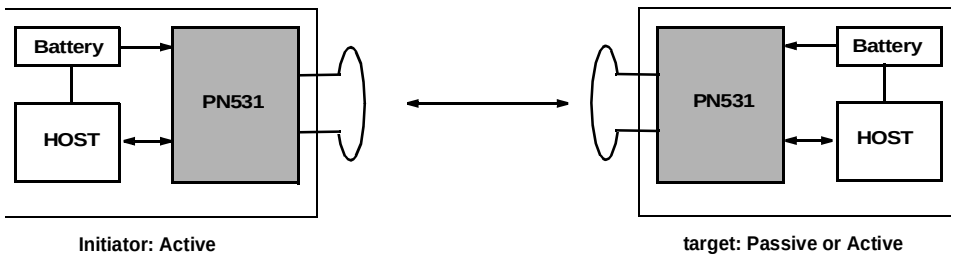


Fig 44. NFCIP-1 Mode

Initiator: generates RF field @ 13.56 MHz and starts the NFCIP-1 communication.

target: responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).

All NFCIP-1 devices shall have communication capability on 106kbps of Type-A encoded bits and may switch to other baudrates or stay at 106kbps.

All NFCIP-1 devices shall have communication capability on 212kbps of FeliCa encoded bits and may switch to other baudrates or stay at 212kbps.

All NFCIP-1 devices shall have communication capabilities on 424kbps of FeliCa encoded bits and may switch to other baudrates or stay at 424kbps.

9.15.3.1 ACTIVE NFCIP-1 mode

Active NFCIP-1 Mode means both the initiator and the target are using their own RF field to enable the communication.

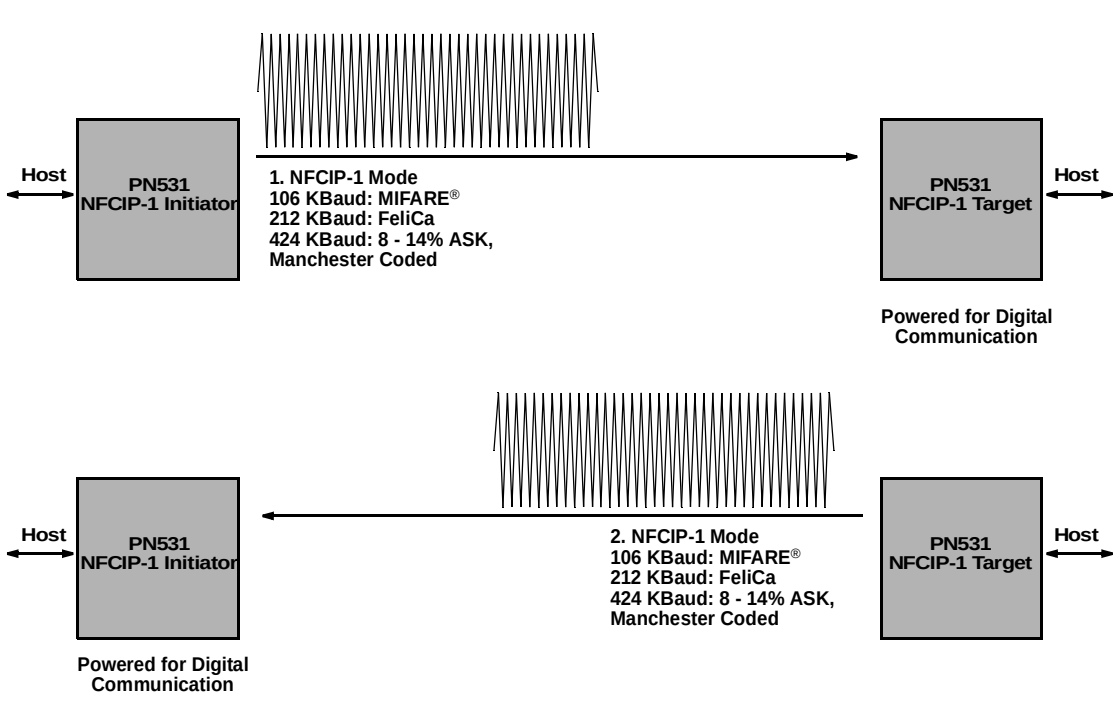


Fig 45. Active NFCIP-1 Mode

Table 173: Communication Overview for active NFCIP-1

Communication direction	106 KBaud	212 KBaud	424 KBaud	848 KBaud	1.69 MBaud 3.39 MBaud
Initiator -> Target	According to ISO/IEC 14443A 100% ASK, Miller Coded	According to FeliCa, 8-14%ASK Manchester Coded	According to FeliCa, 8-14%ASK Manchester Coded	digital capability to handle this communication according to the NFCIP-1 mode	
Target -> Initiator	According to ISO/IEC 14443A 100% ASK, Miller Coded	According to FeliCa, 8-14%ASK Manchester Coded	According to FeliCa, 8-14%ASK Manchester Coded	digital capability to handle this communication according to the NFCIP-1 mode	

In the reader/writer mode the Contact less UART enables the communication to a passive ISO/IEC 14443 A or FeliCa card.

9.15.3.2 PASSIVE NFCIP-1 mode

Passive NFCIP-1 Mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active meaning generating the RF field.

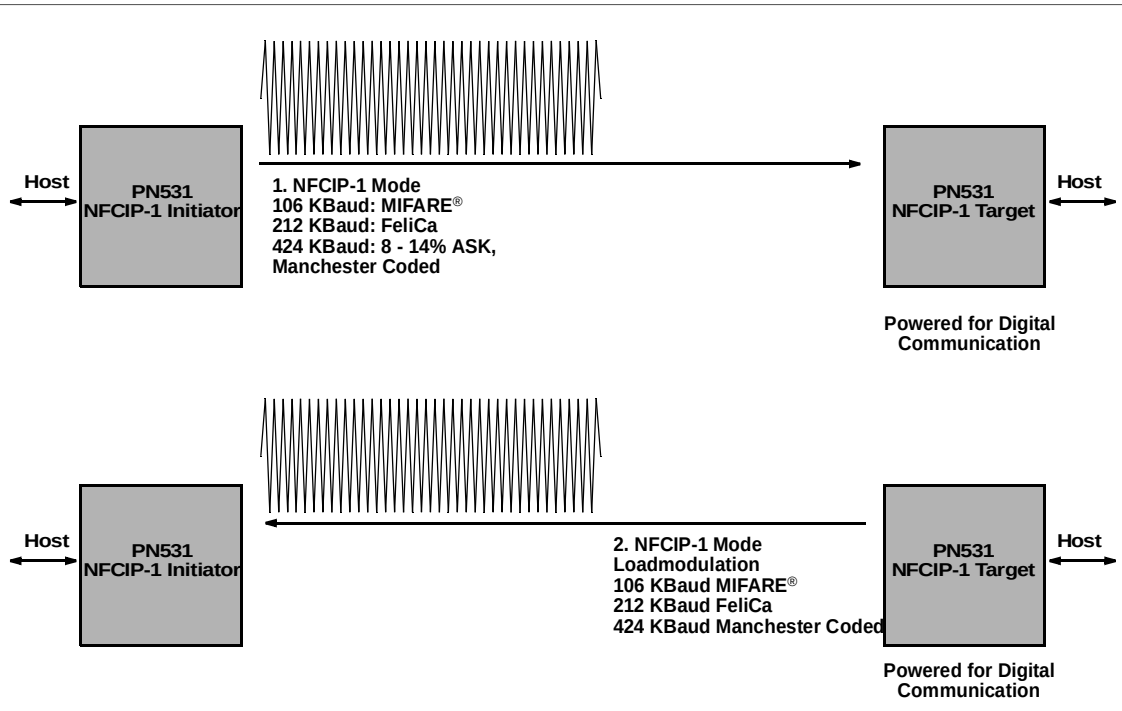


Fig 46. Passive NFCIP-1 Mode

Table 174: Communication Overview for passive NFCIP-1

Communication direction	106 KBaud	212 KBaud	424 KBaud	848 KBaud	1.69 MBaud 3.39 MBaud
Initiator -> Target	According to ISO/IEC 14443A 100% ASK, Miller Coded	According to FeliCa, 8-30%ASK Manchester Coded	According to FeliCa, 8-30%ASK Manchester Coded	digital capability to handle this communication according to the NFCIP-1 mode	
Target -> Initiator	according to ISO/IEC 14443 A subcarrier load modulation, Manchester Coded	according to FeliCa, >12% ASK, Manchester Coded	according to FeliCa, >12% ASK, Manchester Coded	digital capability to handle this communication according to the NFCIP-1 mode	

9.15.3.3 NFCIP-1 FRAMING AND CODING

The active and passive NFCIP-1 framing and coding is defined in the following way:

Table 175: NFCIP-1 Framing and Coding Overview

Baudrate	Framing and Coding
106 KBaud	According to the ISO/IEC 14443 A scheme
212 KBaud	According to the FeliCa scheme
424 KBaud or higher	According to the FeliCa scheme

9.15.3.4 NFCIP-1 Protocol Support

The NFCIP-1 protocol is not completely described in this document, however the datalink layer is according to the following policy:

- Speed shall not be changed while continuum transaction.
- More than one transaction at a time in the same operation field is prohibited.
- Transaction includes initialisation and anticollision methods and data exchange (in continuos way, meaning no interruption by another transaction).

In order not to disturb current infrastructure based on 13.56 MHz general rules to start NFCIP-1 communication are defined in the following way.

- The RF level detector (High level) is active in target mode
- Initiator shall only switch on RF if no external RF field is detected by RF Level detector (low level)
- Only if application requires the NFCIP-1 device shall switch to initiator mode
- The initiator performs the collect UID command in order to select only one NFCIP-1 device for a proper communication.
- Having selected the NFCIP-1 device the used baudrate might be changed to a different one.
- The application starts the data exchange based on the NFCIP-1 protocol

Collect UID command is different according to the baudrates and the NFCIP-1 mode used.

9.15.4 Card Interface mode

The PN531 can be addressed like a FeliCa or ISO/IEC 14443A / MIFARE® card. This means that the PN531 generate an answer in a load modulation scheme according to the ISO/IEC 14443A / MIFARE® or FeliCa interface description.

Remark: The PN531 does not support a complete card protocol. This has to be handled by a dedicated card SAM or a µ-controller. The SAM is optional.

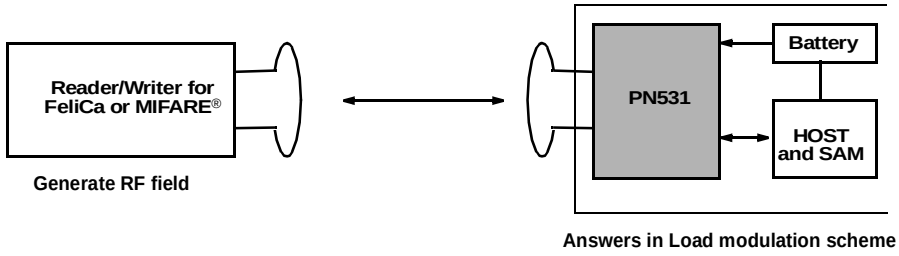


Fig 47. CARD Operating Mode

9.15.4.1 MIFARE® card interface mode

Table 176: MIFARE® CARD operating mode

Communication direction		MIFARE® / ISO/IEC 14443A	MIFARE® Higher Baudrates	
	Baudrate	106 KBaud	212 KBaud	424 KBaud
PN531 receiving data from the reader	Modulation on reader side	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
	Bitlength	9.44 ms	9.44 ms / 2	9.44 ms / 4
PN531 sending data back to the reader	Modulation on PN531 side	Subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	Subcarrier frequency	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16
	bit coding	Manchester coding	BPSK	BPSK

9.15.4.2 FeliCa card interface mode

Table 177: MIFARE® CARD operating mode

Communication direction	Baudrate	FeliCa 212 KBaud	FeliCa Higher Baudrates 424 KBaud
PN531 receiving data from the reader	Modulation on reader side	8-30% ASK	8-30% ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) ms	(64/13.56) ms
PN531 sending data back to the reader	Modulation on PN531 side	>12% ASK, load modulation	>12% ASK, load modulation
	bit coding	Manchester coding	Manchester coding

9.15.5 CRC-Coprocessor

For the CRC-Coprocessor the following parameters may be configured.

Table 178: CRC-Coprocessor Parameters

PARAMETER	VALUE
CRC Register Length	16 Bit CRC
CRC Algorithm	Algorithm according ISO14443A or CCITT
CRC Preset Value	Any

The CRC polynomial for the 16-bit CRC is fixed to x16 + x12 + x5 + 1.

The CRC coprocessor is configurable to handle the different MSB and LSB requirements for the different protocols.

9.15.6 CL UART Block Diagram

The contactless UART is the odule integrated between the CPU and the Contact less analog module.

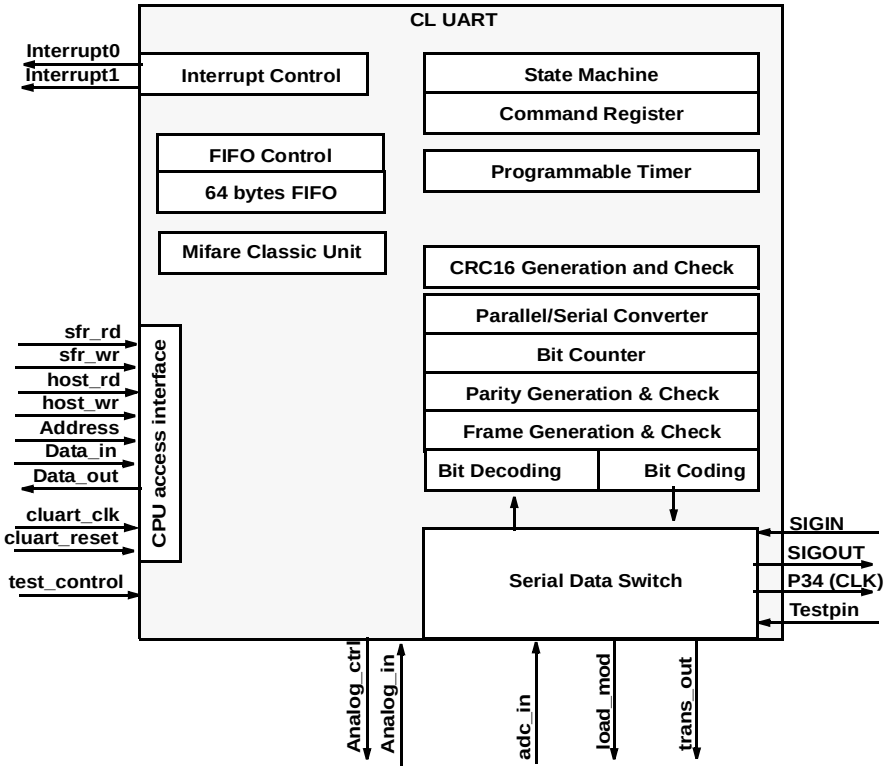


Fig 48. CL UART Block diagram

9.15.7 CL UART Functional Description

The PN531 supports different contactless communication modes at different baudrates from 106 to 424 KBaud.

- Card operating mode
- Reader/Writer operating mode
- NFCIP-1 mode

The integrated contactless UART supports the online with framing and error checking for protocol requirements for the different selected communication schemes as card interface mode, reader /writer operating mode or NFCIP-1 mode up to 424 kbit/s according to the NFCIP-1 standard.

Higher transfer speeds up to 3.39 MBaud can be handled by the contactless UART. To modulate and demodulate the data an external circuit has to be connected to the communication interface SIGIN/SIGOUT.

The contactless UART handles the protocol requirements for the communication schemes in co-operation with the microcontroller. The protocol handling itself generates bit- and byte-oriented framing and handles error detection as Parity & CRC for the different contactless communication schemes.

Notes: The size and the tuning of the antenna have an important impact on the achievable operating distance.

9.15.7.1 TX Driver

The signal delivered on pin TX1 and pin TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly, using a few passive components for matching and filtering, see Section 15 “Application information” on page 198. The signal on TX1 and TX2 can be configured by the register TxControlReg, see Table 225 “CL UART TxControl Register” on page 162.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured by the registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured by the register GsNReg. Furthermore, the modulation index depends on the antenna design and tuning.

The register TxModeReg and TxAutoSelReg control the transmission data rate and framing during the transmission and the setting of the antenna driver to support the different requirements at the different modes and transfer speeds.

Table 179: Settings for TX1

TX1RFEn	Force 100 ASK	InVTx1	Envelope	TX1	GSPMos	GSNMos	Remarks
0	X	0	0	0		nMod	If TX1RFEN=0, the pin TX1 is set to 0 or 1 depending on InvTx1. The bit Force 100ASK has no effect, envelope modulates GS value
0	X	0	1	0		nCW	
0	X	1	0	1	pMod		
0	X	1	1	1	PCW		
1	0	0	0	RF	pMod	nMod	
1	0	0	1	RF	pCW	nCW	
1	1	1	0	0	pMod	nMod	100% ASK: TX1 pulled to 0, independent of InvTxRFoff
1	1	1	1	RF_n	pCW	nCW	

Table 180: Settings for TX2

TX2RFEn	Force 100 ASK	TX2CW	InVTx2	Envelope	TX2	GSPMos	GSNMos	Remarks
0	X	0	0	0	0		nMod	If TX2RFEN=0, the pin TX2 is set to 0 or 1 depending on InvTx1. The bit Force 100ASK has no effect, envelope modulates GS values
0	X	0	0	1	0		nCW	
0	X	0	1	0	1	pMod		
0	X	0	1	1	1	PCW		
0	X	1	0	0	0		nCW	TX2CW: always gsCw values
0	X	1	0	1	0		nCW	
0	X	1	1	0	1	pCW		
0	X	1	1	1	1	pCW		
1	0	0	0	0	RF	pMod	nMod	
1	0	0	0	1	RF	pCW	nCW	
1	0	0	1	0	RF_n	pMod	nMod	
1	0	0	1	1	RF_n	pCW	nCW	
1	0	1	0	X	RF	pCW	pCW	Gs always CW for TX2CW
1	0	1	1	X	RF_n	pCW	pCW	
1	1	0	0	0	0	pMod	pMod	100%ASK:Tx2 pulled to 0 (independent of InvTx2RFOn/InvTx2RFOff)
1	1	0	0	1	RF	pCW	pCW	
1	1	0	1	0	0	pMod	pMod	
1	1	0	1	1	RF_n	pCW	pCW	
1	1	1	0	X	RF	pCW	pCW	
1	1	1	1	X	RF_n	pCW	pCW	

The following abbreviations are used:

- RF: 13. 56 MHz clock derived from 27.12 MHz quartz divided by 2
- RF_n: inverted 13.56 MHz clock
- GsPMos: Conductance, configuration of the PMOS array
- GsNMos: Conductance, configuration of the NMOS array

- pCW: PMOS conductance value for continuos wave defined by CWGsP register
- pMod: PMOS conductance value for modulation defined by ModGsP register
- nCWOn: NMOS conductance value for continuos wave defined by CWGsNOn bits in the GsNOn register
- nModOn: NMOS conductance value for modulation defined by ModGsNOn bits in the GsNOn register
- nCWOff: NMOS conductance value for continuos wave defined by CWGsNOff bits in the GsNOff register
- nModOff: NMOS conductance value for modulation defined by ModGsNOff bits in the GsNOff register

Note: If only 1 driver is switched on, the values for ModGsNOn and CWGsNOn are used for both drivers. It is not possible to have (ModGsNOn and ModGsNOff) or (CWGsNOn and CWGsNOff) active at the same time.

9.15.7.2 RF level detector

The RF level detector is integrated to fulfill NFCIP-1IP1 protocol requirements (e.g. RF collision avoidance).

Furthermore the RF level detector can be used to wake-up the PN531 and to generate an interrupt.

The sensitivity of the RF level detector is adjustable in a 4-bit range using the bits RFLevel in register RFCfgReg.The sensitivity itself depends on the antenna configuration and tuning.

Possible sensitivity levels at the RX pin are listed in the table below:

Table 181: Setting of the RF level detector

VRX [VPP]	RF LEVEL VALUE
~2	1111
~1.4	1110
~0.99	1101
~0.69	1100
~0.49	1011
~0.39	1010
~0.24	1001
~0.17	1000
~0.12	0111
~0.083	0110
~0.058	0101
~0.041	0100
~0.029	0011
~0.020	0010
~0.014	0001
~0.010	0000

To increase the sensitivity of the RF level detector an amplifier can be activated by setting the bit RFLevelAmp in register RFCfgReg to ONE.

Note1: During soft Power-down mode the RF level detector amplifier is automatically switched off to ensure that the power consumption is less than 10 μA @ 3V.

Note2: With typical antennas lower sensitivity levels can lead to misleading results because of intrinsic noise in the environment.

Note3: It is recommended to use the RFLevelAmp only with upper RF level settings.

9.15.7.3 Data Mode Detector

The data mode detector gives the possibility to detect received signals according to the ISO/IEC 14443A / MIFARE®, FeliCa or NFCIP-1 schemes and the standard baudrates for 106 kbit/s, 212 kbit/s and 424 kbit/s in order to prepare the internal receiver in a fast and convenient way.

The data mode detector can only be activated by the AutoColl command. The mode detector is reset, when no external RF field is detected by the RF level detector.

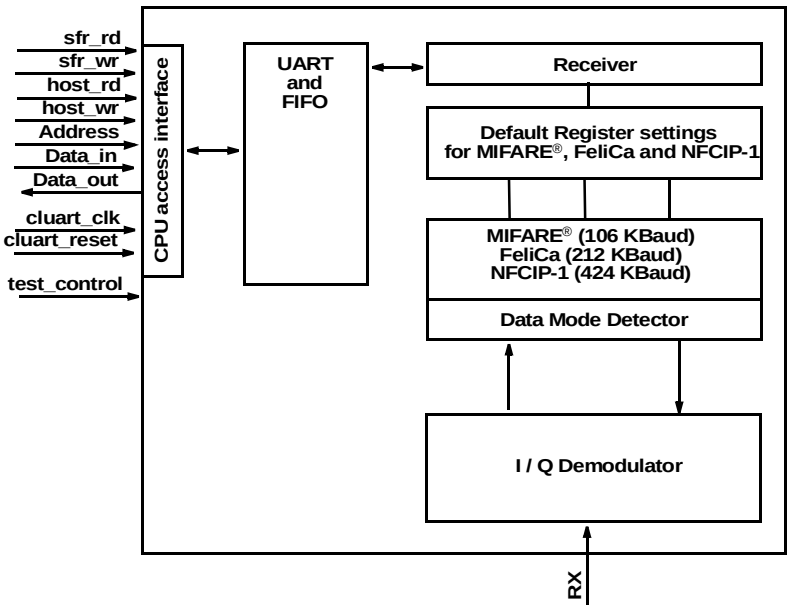


Fig 49. Data mode detector

9.15.7.4 Serial Data Switch

Two main blocks are implemented in the contactless UART. A digital circuitry, comprising state machines, coder and decoder logic and an analog circuitry with the modulator and antenna drivers, receiver and amplification circuitry. The interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins SIGIN and SIGOUT. SIGIN can receive a digital NFCIP-1 signal on transfer speeds above 424kbit/s. The SIGOUT pin can provide a digital signal that can be used with an additional external circuit to generate transfer speeds above 424 kbit/s (including 106 and 212 kbit/s). Furthermore SIGOUT and SIGIN can be used in the card SAM mode to emulate a card functionality with the contactless UART and a secure memory IC.

The LOADMOD pin can be to provide a digital signal to ensure an answer in the card operating mode. This digital signal has to be connected to an external circuitry performing the load modulation at the antenna.

Note: The contactless UART has also internal capability to generate a load modulated signal.

The serial signal switch is controlled by the register TxSelReg and RxSelReg.

9.15.7.5 Serial Data Switch for Driver and Loadmod

The following figure shows the serial data switch for TX1 and TX2.

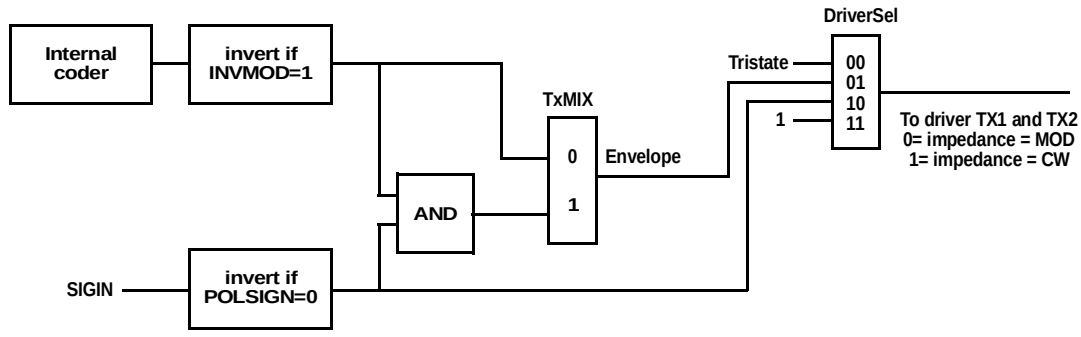


Fig 50. Serial data switch for TX1 and TX2

Pin SIGIN is in general only used for SAM communication. If TxMix is set to ONE, the driver pins are simultaneously controlled by SIGIN and the internal coder.

The following figure shows the serial data switch for the LOADMOD pin.

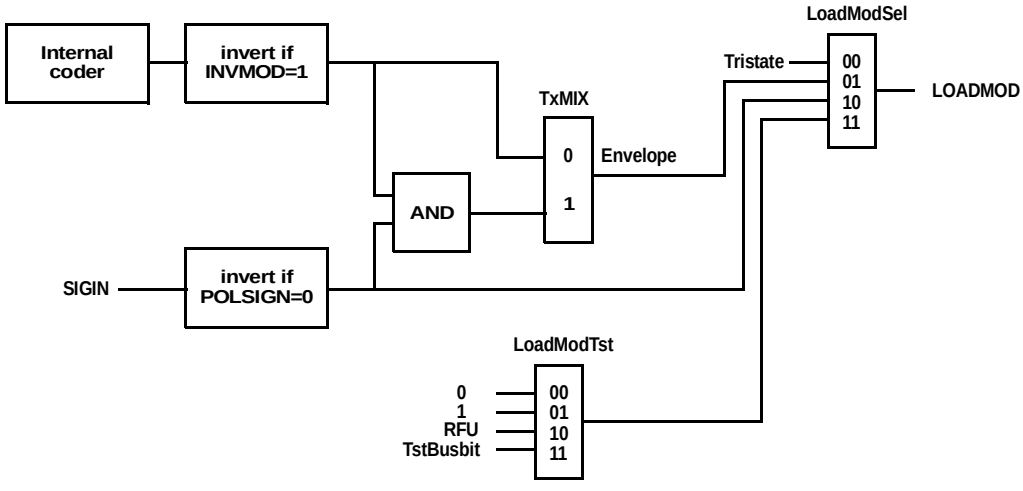


Fig 51. Serial data switch for LOADMOD pin

9.15.7.6 Signal Shape for FeliCa S²C interface support

The FeliCa secure memory IC is connected to the PN531 via the Pins SIGOUT and SIGIN.

The signal at SIGOUT contains the information of the 13.56 MHz clock and the demodulated signal. This signal is a digital signal. The clock and the demodulated signal is combined by using the logical function exclusive or.

To ensure, that this signal is spike free, the demodulated signal is digitally filtered first. The time delay for that digital filtering is in the range of one bit length. The demodulated signal changes only at a positive edge of the clock.

The register TxSelReg controls the setting at SIGOUT

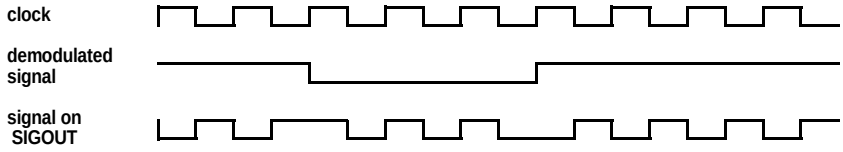


Fig 52. Signal Shape for SIGOUT in FeliCa card SAM mode

The answer of the FeliCa SAM is transferred from SIGIN directly to the antenna driver. The modulation is done according to the register setting of the antenna driver.

The clock is switched to AUX1 or AUX2 (see AnalogSelAux).

Note: A HIGH signal on AUX1 and AUX2 has the same level as AVDD. A HIGH signal at SIGIN and SIGOUT have the same level as SVDD.
Alternatively it is possible to use pin P34 as clock output if a serial interface is used. The HIGH level at P34 is the same as SVDD.

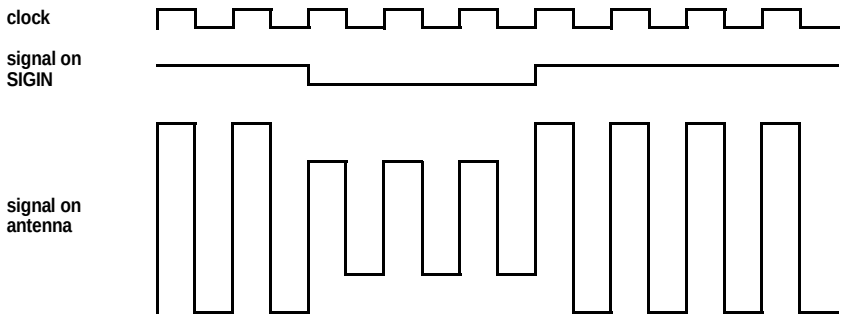


Fig 53. Signal Shape for SIGIN in FeliCa card SAM mode

Note: The signal on antenna is shown in principle only. This signal is sinusoidal. The clock for SIGIN is the same as the clock for SIGOUT.

9.15.7.7 Signal Shape for ISO/IEC14443A and MIFARE® S²C support

The secure core IC, e.g. the Smart MX is connected to the PN531 via the pins SIGOUT, SIGIN and P34.

The signal at SIGOUT is a digital 13.56 MHz Miller coded signal between PVSS and PVDD.

The register TxSelReg controls the setting at SIGOUT.

Fig 54. Signal Shape for SIGOUT in MIFARE® Card SAM mode

The signal at SIGIN is a digital Manchester coded signal at the subcarrier frequency of 847.5 kHz.

Fig 55. Signal Shape for SIGIN in MIFARE® Card SAM mode

9.15.8 Hardware Support for FeliCa and NFCIP-1 Polling

9.15.8.1 Polling Sequence Functionality for Initiator

1. Timer: The contactless UART has a timer, which can be programmed in a way that the timer generates an interrupt at the end of each timeslot, or if required an interrupt is generate at the end of the last timeslot.
2. The receiver can be configured in a way that it is receiving continuously. In this mode it can receive any number of packages. The receiver is ready to receive directly after the last package has been transmitted.This mode has to be stopped by embedded firmware.
3. The internal UART adds one byte to every received package, before it is transferred into the FIFO-buffer. This byte indicates if the result of the CRC calculation is correct (see bit CRCErr in register ErrReg).
4. The first byte of each package contains the length byte of the package.
   The length of one package is 17 or 19 bytes. (+1 byte CRC-Info). The FIFO has a length of 64 bytes. This means 3 packages can be stored in the FIFO. If more than 3 packages are expected, the host has to read out data from the FIFO, before the FIFO is filled completely. In case of an FIFO-overflow data is lost. (See error flag BufferOvfl).

9.15.8.2 Polling Sequence Functionality for Target

1. To activate the automatic polling in target mode, the AutoColl Command has to be activated.
2. The µ-controller has to configure the contactless UART with the correct polling response parameters for the polling command.
3. The contactless UART receives the polling command send out by an initiator and answers with the polling response. The timeslot is selected automatically (The timeslot itself is randomly generated, but in the range 0 to TSN, which is defined by the polling command). The contactless UART compares the system code, stored in byte 17 and 18 of the Config Command with the system code received with the polling command by an initiator. If the system code is equal, the contactless UART answers according to the configured polling response. The system code FF (hex) acts as a wildcard for the system code bytes. If the system code does not match no answer is send back by the contactless UART. If a valid command, which is not a Polling command, is received by the contactless UART, no answer is send back and the command AutoColl is stopped. The received packed is stored in the FIFO.

9.15.8.3 Additional Hardware Support for FeliCa and NFCIP-1

Additionally to the polling sequence support for the FeliCa mode, the contactless UART supports the check of the len-byte.

The received len-byte is checked by the registers FelNFCIP-11Reg and FelNFCIP-12Reg:

DataLenMin in register FelNFCIP-11Reg defines the minimum length of the accepted packet length. This register is 6 bit long. Each value represents a length of 4.

DataLenMax in register FelNFCIP-12Reg defines the maximum length of the accepted package. This register is 6 bit long. Each value represents a length of 4. If set to zero this limit is switched off. If the length is not in the supposed area, the packed is not transferred to the FIFO.

Example 1:
DataLenMin=4: The length shall be greater or equal 16.
DataLenMax=5: The length shall be smaller than 20. Valid area: 16,17,18,19

Example 2:
DataLenMin=9: The length shall be greater or equal 36.
DataLenMax=0: The length shall be smaller than 256. Valid area: 36..255

The data mode detector can be switched off during the Autocall command by setting the bit ModeDetOff in the register mode to logic 1.

9.15.9 Hardware Support for FeliCa and NFC Polling

9.15.9.1 Polling Sequence Functionality for Initiator

1. Timer: The contactless UART has a timer, which can be programmed in a way that the timer generates an interrupt at the end of each timeslot, or if required an interrupt is generate at the end of the last timeslot.
2. The receiver can be configured in a way that it is receiving continuously. In this mode it can receive any number of packages. This mode is activated by the bit RxMultiple in the register RxModeReq to logic 1 and has to be stopped be embedded firmware.
3. The internal UART adds one byte to every received package, before it is transferred into the FIFO-buffer. This byte indicates if the result of the CRC calculation is correct.(see bit CRCErr in register ErrReg). The first byte of each package contains the length byte of the package.
4. The length of one package is 18 or 20 bytes. (+1 byte CRC-Info). The FIFO has a length of 64 bytes. This means 3 packages can be stored in the FIFO. If more than 3 packages are expected, the host has to read out data from the FIFO, before the FIFO is filled completely. In case of an FIFO-overflow data is lost. (See error flag BufferOvfl).

9.15.9.2 Polling Sequence Functionality for Target

1. The µ-controller has to configure the contactless UART with the correct polling response parameters for the polling command.
2. To activate the automatic polling in target mode, the AutoColl Command has to be activated.
3. The contactless UART receives the polling command sent out by an initiator and answers with the polling response. The timeslot is selected automatically (The timeslot itself is randomly generated, but in the range 0 to TSN, which is defined by the polling command). The contactless UART compares the system code, stored in byte 17 and 18 of the Config Command with the system code received with the polling command by an initiator. If the system code is equal, the contactless UART answers according to the configured polling response. The system code FF (hex) acts as a wildcard for the system code bytes, i.e. a target after system code 1234 (hex) answers to the polling command with one of the following system codes 1234 (hex), 12FFh, FF34h or FFFFh. If the systemcode does not match no answer is send back by the contactless UART. If a valid command, which is not a Polling command, is received by the contactless UART, no answer is send back and the command AutoColl is stopped. The received packed is stored in the FIFO.

9.15.9.3 Additional Hardware Support for FeliCa and NFC

Additionally to the polling sequence support for the Felica mode, the contactless UART supports the check of the len-byte.

The received len-byte is checked by the registers FelNFC1Reg and FelNFC2Reg:

DataLenMin in register FelNFC1Reg defines the minimum length of the accepted packet length. This register is 6 bit long. Each value represents a length of 4.

DataLenMax in register FelNFC2Reg defines the maximum length of the accepted package. This register is 6 bit long. Each value represents a length of 4. If set to zero this limit is switched off. If the length is not in the supposed area, the packed is not transferred to the FIFO.

Example 1:
DataLenMin=4: The length shall be greater or equal 16.
DataLenMax=5: The length shall be smaller than 20. Valid area: 16,17,18,19

Example 2:
DataLenMin=9: The length shall be greater or equal 36.
DataLenMax=0: The length shall be smaller than 256. Valid area: 36..255

9.15.10 CRC co-processor

For the CRC co-processor the following parameters may be configured.

Table 182: CRC co-processor Parameters

PARAMETER	VALUE
CRC Register Length	16 bit CRC
CRC Algorithm	Algorithm according ISO/IEC 14443A or CCITT
CRC Preset Value	0000, 6363,A671 or FFFF depending on the CRCPresetReg register settings

The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$.

The CRC co-processor is configurable to handle the different MSB and LSB requirements for the different protocols.

The following register allow the configuration of the CRC co-processor:

CRCPresetReg defines the preset value of the CRC co-processor. Only the values 0000, 6363, A671 or FFFF can be chosen by the CRCPresetReg register.

CRCResultReg indicates the result of the CRC calculation. This register is split into 2 8-bit registers indicating the MSB and LSB byte.

MSBFirst in the register ModeReg indicates that data is loaded with MSB first.

9.15.11 FIFO Buffer

An 64*8 bit FIFO buffer is implemented in the contactless UART. It buffers the input and output data stream between the host µ-Controller and the internal state machine of the contactless UART. Thus, it is possible to handle data streams with lengths of up to 64 bytes without taking timing constraints into account.

9.15.11.1 Accessing the FIFO Buffer

The FIFO-buffer input and output data bus is connected to the register FIFODataReg. Writing to this register stores one byte in the FIFO-buffer and increments the internal FIFO-buffer write-pointer. Reading from this register shows the FIFO-buffer contents stored at the FIFO-buffer read-pointer and decrements the FIFO-buffer read-pointer. The distance between the write- and read-pointer can be obtained by reading the register FIFOLevelReg.

When the microcontroller starts a command, the contactless UART may, while the command is in progress, access the FIFO-buffer according to that command. Physically only one FIFO-buffer is implemented, which can be used in input- and output direction. Therefore the microcontroller has to take care, not to access the FIFO-buffer in an unintended way.

9.15.11.2 Controlling the FIFO-Buffer

Besides writing to and reading from the FIFO-buffer, the FIFO-buffer pointers might be reset by setting the bit FlushBuffer in the register FIFOLevelReg. Consequently, the FIFOLevel bits are set to Zero, the bit BufferOvfl in the register ErrorReg is cleared, the actually stored bytes are not accessible anymore and the FIFO-buffer can be filled with another 64 bytes again.

9.15.11.3 Status Information about the FIFO-Buffer

The microcontroller may obtain the following data about the FIFO-buffers status:

- Number of bytes already stored in the FIFO-buffer: FIFOLevel in register FIFOLevelReg
- Warning, that the FIFO-buffer is quite full: HiAlert in register Status1Reg
- Warning, that the FIFO-buffer is quite empty: LoAlert in register Status1Reg
- Indication, that bytes were written to the FIFO-buffer although it was already full: BufferOvfl in register ErrorReg.
  BufferOvfl can be cleared only by setting bit FlushBuffer in the register FIFOLevelReg.

The contactless UART can generate an interrupt signal

- If LoAlertIEn in register CommIEnReg is set to 1 it will activate Pin IRQ when LoAlert in the register Status1Reg changes to 1.
- If HiAlertIEN in register CommIEnReg is set to 1 it will activate Pin IRQ when HiAlert in the register Status1Reg changes to 1.

The flag HiAlert is set to 1 if only WaterLevel bytes (as set in register WaterLevelReg) or less can be stored in the FIFO-buffer. It is generated by the following equation:

$HiAlert = (64 - FIFOLength) \leq WaterLevel$

The flag LoAlert is set to 1 if WaterLevel bytes (as set in register WaterLevelReg) or less are actually stored in the FIFO-buffer. It is generated by the following equation:

$LoAlert = FIFOLength \leq WaterLevel$

9.15.12 Timer Unit

A timer unit is implemented in the contactless UART. The microcontroller use this timer to manage timing relevant tasks for contactless communication. The timer unit may be used in one of the following configurations:

- Time-out-Counter
- Watch-Dog Counter
- Stop Watch
- Programmable One-Shot
- Periodical Trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events which will be explained in the following, but the timer itself does not influence any internal event (e.g. A time-out during data reception does not influence the reception process automatically). Furthermore, several timer related flags are set and these flags can be used to generate an interrupt.

9.15.12.1 Timer

The timer has a input clock of 6.78 MHz (derived from the 27.12 MHz quartz). The timer consists of 2 stages: 1 prescaler and 1 counter.

The prescaler is a full 12 bit counter. The reload value for TPrescaler can be defined between 0 and 4095 in register TModeReg and TPrescalerReg.

The reload value for the counter is defined with 16 bits in a range from 0 to 65535 in the register TReloadReg.

The current value of the timer is indicated by the register TCounterValReg.

If the counter reaches ZERO an interrupt will be generated automatically indicated by setting the TimerIRq flag in the register CommonIRqReg. If enabled, this event can be indicated on the IRQ line. The TimerIRq flag can be set and reset by the host. Depending on the configuration the timer will stop at 0 or restart with the value of the register TReloadReg.

The status of timer is indicated by the bit TRunning in the register Status1Reg.

The timer can be started by TStartNow in register ControlReg or stopped by TStopNow in register ControlReg.

Furthermore the timer can be activated automatically by setting the bit TAuto in the register TModeReg to fulfill dedicated protocol requirements automatically.

The time delay of a timer stage is the reload value +1.

Maximum time: TPrescaler = 4095, TReloadVal = 65535
=> 4096*65536 / 6.78 MHz = 39.59 s

Example: To indicate 100us it is required to count 678 clock cycles. This means the value for TPrescaler has to be set to TPrescaler =677.The timer has now an input clock of 100us. The timer can count up to 65535 timeslots of 100 µs.

9.15.13 Interrupt Request System

The contactless UART indicates certain events by setting bit IRq in the register Status1Reg and, in addition, by activating pin IRQ. The signal on pin IRQ may be used to interrupt the microcontroller using its interrupt handling capabilities. This allows the implementation of efficient microcontroller embedded firmware.

9.15.13.1 Interrupt Sources

The following table shows the integrated interrupt flags, the related source and the condition for its setting.

The interrupt flag TimerIRq in the register CommIRqReg indicates an interrupt set by the timer unit. The setting is done when the timer decrements from 1 down to zero.
The TxIRq bit in the register CommIRqReg indicates if the transmitter is active and the state changes from sending data to transmitting the end of frame pattern, the transmitter unit sets automatically the interrupt bit.

The CRC co-processor sets the flag CRCIRq in the register DivIRqReg after having processed all data from the FIFO buffer. This is indicated by the flag CRCReady = 1.

The RxIRq flag in the register CommIRqReg indicates an interrupt when the end of the received data is detected.

The flag IdleIRq in the register CommIRqReg is set if a command finishes and the content of the command register changes to idle.

The flag HiAlertIRq in the register CommIRqReg is set to 1 if the HiAlert bit is set to one, that means the FIFO buffer has reached the level indicated by the bit WaterLevel.

The flag LoAlertIRq in the register CommIRqReg is set to 1 if the LoAlert bit is set to one, that means the FIFO buffer has reached the level indicated by the bit WaterLevel.

The flag RFOnIRq in the register DivIRqReg is set to one when the RF level detector detects an external RF field.

The flag RFOffIRq in the register DivIRqReg is set to one, when a present external RF field is switched off.

The flag ErrIRq in the register CommIRqReg indicates an error detected by the contactless UART during sending or receiving.

The flag ModeIRq in the register DivIRqReg indicates that the data mode detector has detected the current mode.

Table 183: High priority Interrupt sources

Interrupt Flag	Interrupt source	Set automatically, WHEN
TxIRq	Transmitter	a transmitted data stream ends
RxIRq	Receiver	a received data stream ends
HiAlertIRq	FIFO-buffer	the FIFO-buffer is getting full
LoAlertIRq	FIFO-buffer	the FIFO-buffer is getting empty

Table 184: Low priority Interrupt sources

Interrupt Flag	Interrupt source	Set automatically, WHEN
TimerIRq	Timer Unit	the timer counts from 1 to 0
CRCIRq	CRC co-processor	all data from the FIFO buffer has been processed
IdleIRq	Command Register	a command execution finishes
RFOnIRq	RF Level Detector	an external RF field is detected
RFOffIRq	RF Level Detector	a present external RF field is switched off
ErrIRq	contactless UART	an error is detected
ModeIRq	data mode detector	the mode has been detected

9.15.14 Contactless UART Power Reduction Modes

9.15.14.1 Hard Power Down

A Hard Power Down is enabled when RSTPD is asserted. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pads and defined internally. The output pins are frozen at a certain value

The RF level detector is not working.

9.15.14.2 Soft Power Down

The Soft Power Down-mode is entered immediately by setting the Power-down bit in the register CommandReg of the contactless UART. All internal current sinks are switched off except the 27.12 MHz oscillator.

In difference to the Hard Power Down-mode, the digital input-buffers are not separated by the input pads and keep their functionality. The digital output pins do not change their state

All registers and the FIFO will keep the content during Soft Power Down.

The RF level detector is working.

If the bit AutoWakeUp in the register TxAutoReg is set and an external RF field is detected, the Soft Power Down mode is be left automatically.

After resetting bit Power-down in the register CommandReg it needs few clocks cycle until the Soft Power Down mode is left indicated by the Power-down bit itself. Resetting it does not immediately clear it. It is cleared automatically by the contactless UART when the Soft Power Down-Mode is left.

9.15.14.3 Transmitter Power Down

The Transmitter Power Down mode switches off the internal antenna drivers to turn off the RF field by setting a specific register bit. The receiver is still switched on, meaning the contactless UART can be accessed by a second one as a target.

9.15.15 CL UART Command Set

9.15.15.1 General Description

The contactless UART behaviour is determined by an internal state machine capable to perform a certain set of commands. Writing the according command-code to the Command-Register can start the commands.

Arguments and/or data necessary to process a command are mainly exchanged via the FIFO buffer.

9.15.15.2 General Behaviour

- Each command, that needs a data stream (or data byte stream) as input will immediately process the data it finds in the FIFO buffer.
- Each command that needs a certain number of arguments will start processing only when it has received the correct number of arguments via the FIFO buffer.
- The FIFO buffer is not cleared automatically at command start. Therefore, it is also possible to write the command arguments and/or the data bytes into the FIFO buffer and start the command afterwards.
- Each command may be interrupted by the microcontroller by writing a new command code into the Command-Register e.g.: the Idle-Command.

9.15.15.3 Commands Overview

Table 185: Command Overview

Command	Command Code	Action
Idle	0000	No action; cancels current command execution.
Config	0001	Configures the contactless UART for FeliCa, MIFARE® and NFCIP-1 communication
Generate RandomID	0010	Generates a 10 bytes random ID number
CalcCRC	0011	Activates the CRC co-processor or perform selftest.
Transmit	0100	Transmits data from the FIFO buffer.
NoCmdChange	0111	No command change. This command can be used to modify different bits in the command register without touching the command. E.G. Power down.
Receive	1000	Activates the receiver circuitry.
Transceive	1100	If bit Initiator in the register ControlReg is set to 1: Transmits data from FIFO buffer to the antenna and activates automatically the receiver after transmission. If bit Initiator in the register ControlReg is set to 0 Receives data from antenna and activates automatically the transmitter.
AutoColl	1101	Handles FeliCa polling (card interface mode only) and MIFARE® anticollision (card interface mode only)
MFAuthent	1110	performs the MIFARE® standard authentication as a reader
Soft Reset	1111	resets the contactless UART

9.15.15.4 Idle Command

The contactless UART is in idle mode. This command is also used to terminate the actual command.

9.15.15.5 Config Command

To configure the automatic MIFARE® Anticollision, FeliCa Polling and the used NFCIP-1ID the following data have to be written to the FIFO:

- SENS_RES (2 bytes), NFCIP-1ID1 (3 bytes), SEL_RES (1 byte)
- polling response (2 bytes + 6 bytes NFCIP-1ID2 + 8 bytes Pad + 2 bytes system code)
- NFCIP-1ID3 (1 byte)

In total 25 bytes. These bytes are transferred into an internal buffer.

The NFCIP-1ID3 is 10 bytes long and consist of the 3 NFCIP-1ID1 bytes, the 6 NFCIP-1ID 2 bytes and the last send NFCIP-1IP 3 bytes.

To read out this configuration the command Config with an empty FIFO buffer has to be started. In this case the 25 bytes are transferred from the internal buffer to the FIFO.

The contactless UART has to be configured after each powering up, before using the automatic Anticollision/Polling function (AutoColl). During a hard power-down (reset pin) this configuration remains unchanged.

This command terminates automatically when finished.

9.15.15.6 Generate RandomID Command

This command generates internally a 10 bytes random number. This random number might be used for the automatic Anticollision/Polling function.

Note: To configure the contactless UART the command Config has to be used first. Using the command GenerateRandomID the actual value for the ID will be overwritten.

This command terminates automatically when finished.

9.15.15.7 CalcCRC Command

The content of the FIFO is transferred to the CRC co-processor. The result is stored in the CRCResult register. The CRC can be calculated of every amount of bytes by transferring all data into the FIFO. The calculation is not stopped, when the FIFO gets empty during the data stream.

The preset value of the CRC is loaded from the CRCPreset register to the CRC co-processor when the command is started.

This command has to be cleared by embedded firmware by writing any command to the Command-register e.g. the command idle.

If the bit SelfTest is set to 1, the CRC co-processor is in self test mode and performs a digital selftest. The result of the selftest is written in the FIFO.

9.15.15.8 Transmit Command

The content of the FIFO is transmitted. Before transmitting FIFO content all relevant register settings have to be made.

This command terminates automatically when the FIFO gets empty.

9.15.15.9 Receive Command

The contactless UART activates the receiver and wait for any data stream. The demodulation, framing, CRC checking, etc. can be chosen by the register.

This command terminates automatically when receiving data stream is finished, except when the Register RxMultiple is chosen.

9.15.15.10 Transceive Command

This command is one endless stream of transmitting data from the FIFO and receiving data from the RF field. The bit Initiator in the register ControlReg indicates whether the first action is transmitting (Initiator =1) or receiving (Initiator=0).

- Initiator =1.... Initiator=0...
- Send .....Receive.....
- Receive..... Send.....
- Send..... Receive.....
- Receive ….....Send ..…

Each transmitting process has to be started with setting bit StartSend in the register BitFramingReg. This command has to be cleared by embedded firmware by writing any command to the Command-register e.g. the command idle.
Note: If the bit RxMultiple in register RxModeReg is set, this command will never leave the receiving state, because the receiving will not be cancelled.

9.15.15.11 AutoColl Command

This command handles the MIFARE® anticollision and the FeliCa polling automatically for the target mode. The bit Initiator in the register ControlReg has to be 0. After the mode detector detects the mode, the registers are set according the received mode. In case of no external RF field this command returns to the initial state but it will not be terminated.

- TP 106 passive:This command is changing automatically to the command Transceive when the MIFARE® anticollision is finished. The FIFO contains the ATR REQ.
- TP 212/424 passive:This command is changing automatically to the command Transceive when the FeliCa polling is finished. The FIFO contains the ATR REQ
- TP 106/212/424 active:This command is changing automatically to the command Transceive. The FIFO contains the ATR REQ
- MIFARE®:This command is changing automatically to the command Transceive when the MIFARE® anticollision is finished. The FIFO contains the command followed by the Select.
- FeliCa:This command is changing automatically to the command Transceive when the FeliCa polling is finished. The FIFO contains the command followed by the Polling.

9.15.15.12 MFAuthent Command

This command handles the MIFARE® authentication in reader/writer mode. The following data shall be written to the FIFO before the command can be activated:

- authentication command code (60h, 61h)
- Block address
- sector key byte 0
- sector key byte 1
- sector key byte 2
- sector key byte 3
- sector key byte 4
- sector key byte 5
- card serial number byte 0
- card serial number byte 1
- card serial number byte 2
- card serial number byte 3

In total 12 bytes shall be written to the FIFO.
Note: During active MFAuthent command, any FIFO access is blocked.

This command terminates automatically when the MIFARE® card is authenticated. This command terminates not automatically when the card does not answer (Use Timer for Time-Out). In case of wrong data the protocol error can be set. The bit Crypto1On in register Status2Reg indicates a successful authentication.

9.15.15.13 SoftReset Command

This command performs a reset to the device. The configuration data of the internal buffer remains unchanged.

This command terminates automatically when finished.

9.15.16 CL UART Tests Signals

9.15.16.1 Selftest

The contactless UART has the capability to perform a selftest. To start the selftest the following procedure has to be performed:

- Perform a soft reset
- Clear the FIFO buffer by writing 25 bytes of 00h and perform the Config Command.
- Enable the Selftest by writing the value 09h to the register AutoTestReg.
- Write 00h in the FIFO.
- Start the Selftest with the CalcCRC Command.
- The Selftest will be performed.
- When the Selftest is finished, the FIFO is contains 64 bytes depending on the version number.

9.15.16.2 Testbus

The testbus is implemented for production test reasons. The following configuration can be used to improve the design of an system using the contactless UART. The testbus allows to route internal signals to the digital interface. The testbus signals are selected by accessing TestBusSel in register TestSel2Reg.

Table 186: TstBusBitSel set to 07

Test signal	Comments
sdata	shows the actual received data value.
scoll	shows if in the actual bit a collision has been detected (106 kbit/s only)
svalid	shows if sdata and scoll are valid
sover	shows that the receiver has detected a stop bit (ISO/IEC 14443 A/MIFARE® mode only)
RCV_reset	shows if the receiver is reset
RFon filtered	shows the value of the internal RF level detector
Envelope	shows the output of the internal coder

Table 187: TstBusBitSel set to 0D

Test signal	Comments
clkstable	shows if the oscillator delivers a stable signal.
clk27/8	shows the output signal of the oscillator divided by 8
clk27rf/8	shows the clk27rf signal divided by 8
clk13/4	shows the clk13rf divided by 4.
clk27	shows the output signal of the oscillator
clk27rf	shows the RF clock multiplied by 2.
clk13rf	shows the RF clock of 13.56 MHz

9.15.16.3 Testsignals at pin AUX

Table 188: Testsignals Description on AUX pins

SELAUX	Description for Aux1 / Aux2
0000	Tristate
0001	DAC: register TestDAC 1/2
0010	DAC: testsignal corr1
0011	DAC: testsignal corr2
0100	DAC: testsignal MinLevel
0101	DAC: ADC_I
0110	DAC: ADC_Q
0111	DAC: testsignal ADC_I combined with ADC_Q
1001	SAM clock
1010	High
1011	low
1100	TxActive
1101	RxActive
1111	TstBusBit

Each signal can be switched to pin AUX1 or AUX2 by setting SelAux1 or SelAux2 in the register AnalogTestReg.

Note: The DAC has a current output, it is recommended to use a 1 kΩ pull-down resistance at AUX1/AUX2.

9.15.16.4 PRBS

Enables the PRBS9 or PRBS15 sequence according to ITU-TO150. To start the transmission of the defined datastream the command send has to be activated. The preamble / Sync byte /start bit / parity bit are generated automatically depending on the selected mode.
Note: All relevant register to transmit data have to be configured before entering PRBS mode according ITU-TO150.

9.15.17 Contact Less Memory Map

The registers of the Contact Less UART are either map into the SFR or into the XRAM memory space.

Table 189: CL UART SFR memory map

Physical Address	Size (bytes)	Register Name	Description
D1h	1	Command	Starts and stops the command execution
D2h	1	CommIEn	Controls bits to enable and disable the passing of interrupt requests
D3h	1	DivlEn	Controls bits to enable and disable the passing of interrupt requests
D4h	1	CommIrq	Contains common Interrupt Request flags
D5h	1	DivIrq	Contains diverse Interrupt Request flags
D6h	1	Error	error flags showing the error status of the last command executed
DFh	1	Status1	Contains status flags of the CRC, Interrupt and FIFO buffer
E9h	1	Status2	Contain status flags of the receiver, transmitter and data mode detector
EAh	1	FIFOData	in- and output of 64 bytes FIFO buffer
EBh	1	FIFOLevel	Indicates the number of bytes stored in the FIFO
ECh	1	WaterLevel	Defines the level for FIFO under- and overflow warning
hED	1	Control	Diverse Control Register
EEh	1	BitFraming	Adjustments for bit oriented frames
EFh	1	Coll	bit position of the first bit collision detected on the RF-interface

Table 190: CL UART Extension memory map

Physical Address	Size (bytes)	Register Name	Description
6300h	1	SAMClk_en	Enables the use of SAM CLK on P34.
6301h	1	Mode	Defines general modes for transmitting and receiving
6302h	1	TxMode	Defines the transmission data rate and framing during transmission
6303h	1	RxMode	Defines the transmission data rate and framing during receiving
6304h	1	TxControl	controls the logical behaviour of the antenna driver pins TX1 and TX2
6305h	1	TxAuto	controls the settings of the antenna driver
6306h	1	TxSel	Selects the internal sources for the antenna driver
6307h	1	RxSel	Selects internal receiver settings
6308h	1	RxTreshold	Selects thresholds for the bit decoder
6309h	1	Demod	Defines demodulator settings
630Ah	1	FelNFCIP-11	Defines the length of the valid range for the receive package
630Bh	1	FelNFCIP-12	Defines the length of the valid range for the receive package

Table 190: CL UART Extension memory map *…continued*

Physical Address	Size (bytes)	Register Name	Description
630Ch	1	MifNFCIP-1	Controls the communication in ISO/IEC 14443/ MIFARE® and NFCIP-1 target mode at 106 kbit/s
630Dh	1	ManualRCV	Allows manual fine tuning of the internal receiver
630Eh	1	-	Reserved
630Fh	1	-	Reserved
6310h	1	-	Reserved
6311h	1	CRCResultMSB	Shows the actual MSB values of the CRC calculation
6312h	1	CRCResultLSB	Shows the actual LSB values of the CRC calculation
6313h	1	GsNLoadMod	Selects the conductance of the antenna driver pins TX1 and TX2 for load modulation
6314h	1	ModWidth	Controls the setting of the ModWidth
6315h	1	TxBitPhase	Adjust the TX bitphase at 106 kbit/s
6316h	1	RFCfg	Configures the receiver gain and RF level
6317h	1	GsN	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation
6318h	1	CWGsP	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation
6319h	1	ModGsP	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation
631Ah	1	TMode	Defines settings for the internal timer
631Bh	1	TPrescaler	
631Ch	1	TReloadVal_hi	Describes the 16 bit long TReLoad value (Higher 8 bits)
631Dh	1	TReloadVal_lo	Describes the 16 bit long TReLoad value (Lower 8 bits)
631Eh	1	TCounterValue_hi	Describes the 16 bit long timer reload value (Higher 8 bits)
631Fh	1	TCounterValue_lo	Describes the 16 bit long timer reload value (Lower 8 bits)
6320h	1	-	Reserved
6321h	1	TestSel1	General test signal configuration
6322h	1	TestSel2	General test signal configuration and PRBS control
6323h	1	-	Reserved
6324h	1	TestPinValue	Defines the values for the 7 bit parallel bus when it is used as I/O bus
6325h	1	TestBus	Shows the status of the internal testbus
6326h	1	AutoTest	Controls the digital selftest
6327h	1	Version	Shows the version
6328h	1	AnalogTest	Controls the pins AUX1 and AUX2
6329h	1	TestDAC1	Defines the test value for the TestDAC1
632Ah	1	TestDAC2	Defines the test value for the TestDAC2
632Bh	1	TestADC	Show the actual value of ADC I and Q
632Ch	1		Reserved
632Dh	1		Reserved
632Eh	1		Reserved
632Fh	1		Reserved

9.15.18 CL UART Register Description

9.15.18.1 CL UART Register bit behaviour

Bits and flags for different registers behave differently, depending on their functions. In principle bits with same behaviour are grouped in common registers.

Table 191: Behaviour of Register Bits

Abbreviation	Behaviour	Description
r/w	read and write	These bits can be written and read by the microcontroller. Since they are used only for control means, there content is not influenced by internal state machines, e.g. the CommIEnReg may be written and read by the µ-Processor. It will also be read by internal state machines, but never changed by them.
dy	dynamic	These bits can be written and read by the µ-Processor. Nevertheless, they may also be written automatically by internal state machines, e.g. the Command-Register changes its value automatically after the execution of the actual command.
r	read only	These registers hold flags, which value is determined by internal states only, e.g. the CRC Ready-Register can not be written from external but shows internal states.
w	write only	These registers are used for control means only. They may be written by the µ-Processor but can not be read. Reading these registers returns an undefined value.

9.15.18.2 Command Register

Starts and stops the command execution.

Table 192: CL UART Register (address D1h or 6331h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	RcvOff	Power-down	Command			
Reset	X	X	1	0	0	0	0	0
Access			R/W	dy	dy	dy	dy	dy

Table 193: Description of CL UART Register bits

Bit	Symbol	Description
7 to 6	-	Reserved.
5	RcvOff	Set to 1, the analog part of the receiver is switched off.
4	Power-down	Set to 1, the Soft Power-down mode of the CLUART is entered. This means, internal current consuming blocks of the contactless analog module are switched off.Note: Do not set this bit, when you start the command Soft Reset.
3 to 0	Command	Activates a command according the Command Code. Reading this register shows, which command is actually executed. Section 9.15.15 “CL UART Command Set” on page 143.

9.15.18.3 CommIEn Register

Controls bits to enable and disable the passing of interrupt requests.

Table 194: CL UART CommIEn Register (address D2h or 6332h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Reset	X	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 195: Description of CL UART CommIEn Register bits

Bit	Symbol	Description
7	-	Reserved.
6	TxIEn	Allows the transmitter interrupt request (indicated by bit TxIRq) to be propagated to CL_interrupt_1.
5	RxIEn	Allows the receiver interrupt request (indicated by bit RxIRq) to be propagated to CL_interrupt_1.
4	IdleIEn	Allows the idle interrupt request (indicated by bit IdleIRq) to be propagated to CL_interrupt_0.
3	HiAlertIEn	Allows the high alert interrupt request (indicated by bit HiAlertIRq) to be propagated to CL_interrupt_1.
2	LoAlertIEn	Allows the low alert interrupt request (indicated by bit LoAlertIRq) to be propagated to CL_interrupt_1.
1	ErrIEn	Allows the error interrupt request (indicated by bit ErrIRq) to be propagated to CL_interrupt_0.
0	TimerIEn	Allows the timer interrupt request (indicated by bit TimerIRq) to be propagated to CL_interrupt_0.

9.15.18.4 Register DivIEn

Controls bits to enable and disable the passing of interrupt requests.

Table 196: CL UART DivIEn Register (address D3h or 6333h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	SiginAct IEn	ModeIEn	CRCIEn	RfOnIEn	RfOffIEn
Reset	X	X	X	0	0	0	0	0
Access				R/W	R/W	R/W	R/W	R/W

Table 197: Description of CL UART DivIEn Register bits

Bit	Symbol	Description
7 to 5	-	Reserved.
4	SiginAct IEn	Allows the SIGIN active interrupt request to be propagated to CL_interrupt_0.
3	ModeIEn	Allows the mode interrupt request (indicated by bit ModeIRq) to be propagated to CL_interrupt_0.
2	CRCIEn	Allows the CRC interrupt request (indicated by bit CRCIRq) to be propagated to CL_interrupt_0.
1	RfOnIEn	Allows the RF field on interrupt request (indicated by bit RfOnIRq) to be propagated to CL_interrupt_0.
0	RfOffIEn	Allows the RF field off interrupt request (indicated by bit RfOffIRq) to be propagated to CL_interrupt_0.

9.15.18.5 Register CommIRQ

Contains Interrupt Request flags.

Table 198: CL UART CommIRQ Register (address D4h or 6334h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxIRq	RxIRq	IdleIrq	HiAltertIRq	LoAlertIRq	ErrIRq	TimerIRq
Reset	0	0	0	1	0	1	0	0
Access	W	dy	dy	dy	dy	dy	dy	dy

Table 199: Description of CL UART DivIEn Register bits

Bit	Symbol	Description
7	Set1	Set to 1, Set1 defines that the marked bits in the CommIRQ Register are set. Set to 0, Set1 defines that the marked bits in the CommIRQ Register are cleared.
6	TxIRq	Set to 1, immediately after the last bit of the transmitted data was sent out.
5	RxIRq	Set to 1, when the receiver detects the end of a valid datastream. If the bit RxNoErr in register RxModeReg is set to 1, Bit RxIRQ is only set to1 when data bytes are available in the FIFO.
4	IdleIrq	Set to 1, when a command terminates by itself e.g. when the Command Register changes its value from any command to the Idle Command. If an unknown command is started, the command register changes its value to the idle Command and the bit IdleIRq is set. Starting the Idle Command by the microcontroller does not set bit IdleIRq.
3	HiAltertIRq	Set to 1, when bit HiAlert in register Status1reg is set. In opposition to HiAlert, HiAlertIRq stores this event and can only be reset by bit Set1.
2	LoAlertIRq	Set to 1, when bit LoAlert in register Status1reg is set. In opposition to LoAlert, LoAlertIRq stores this event and can only be reset by bit Set1.
1	ErrIRq	Set to 1, if any error flag in the Error Register is set.
0	TimerIRq	Set to 1, when the timer decrements the TimerValue Register to zero.

[1] **Remark:** All bits in the register CommIRqReg shall be cleared by embedded firmware.

9.15.18.6 Register DivIRq

Contains diverse Interrupt Request flags.

Table 200: CL UART DivIRq Register (address D5h or 6335h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set2	-	-	SiginActIrq	ModeIRq	CRCIRq	RfOnIRq	RfOffIRq
Reset	0	X	X	X	0	0	X	X
Access	W	R	R	dy	dy	dy	dy	dy

Table 201: Description of CL UART DivIRq Register bits

Bit	Symbol	Description
7	Set2	Set to 1, Set2 defines that the marked bits in the DivIRq Register are set. Set to 0, Set2 defines that the marked bits in the DivIRq Register are cleared.
6 to 5	-	Reserved.
4	SiginActIrq	Set to 1, when SIGIN is active. This interrupt is set when either a rising or falling signal edge is detected.
3	ModeIRq	Set to 1, when the mode has been detected by the data mode detector. **Remark:** The data mode detector can only be activated by the AutoColl command and is terminated automatically having the detected the communication mode.
2	CRCIRq	Set to 1, when the CRC command is active and all data is processed.
1	RfOnIRq	Set to 1, when an external RF field is detected.
0	RfOffIRq	Set to 1, when an present external RF field is switched off.

[1] **Remark:** All IRq register shall be cleared by embedded firmware.

9.15.18.7 Register Error

Error flag register showing the error status of the last command executed.

Table 202: CL UART Error Register (address D6h or 6336h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	RFErr	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocollErr
Reset	0	X	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 203: Description of CL UART Error Register bits

Bit	Symbol	Description
7	WrErr	Set to 1, when data is written into the FIFO by the microcontroller during the AutoColl command or MFAuthent command or if data is written into the FIFO by the microcontroller during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface.
6	TempErr	Set to 1, if the internal temperature sensor detects overheating. In this case the antenna drivers are switched off automatically.
5	RFErr	Set to 1, if in active communication mode the counterpart does not switch on the RF field in time as defined in NFCIP-1 standard. Note: RFErr is only used in active communication mode. The bit RxFraming or the bit TxFraming has to be set to 1 to enable this functionality.
4	BufferOvfl	Set to 1, if the microcontroller or if the internal state machine (e.g. receiver) tries to write data into the FIFO buffer although the FIFO buffer is already full.
3	CollErr	Set to 1, if a bit-collision is detected. It is cleared automatically at receiver start phase. This flag is only valid during the bitwise anticollsion at 106 kbit/s. During communication schemes at 212 and 424 kbit/s this flag is always set to ZERO.
2	CRCErr	Set to 1, if RxCRCEn in register RxModeReg is set and the CRC calculation fails. It is cleared to 0 automatically at receiver start phase.
1	ParityErr	Set to 1, if the parity check has failed. It is cleared automatically at receiver start phase. Only valid for ISO/IEC 14443A/MIFARE® or NFCIP-1 communication at 106 kbit/s.
0	ProtocollErr	Set to 1, if one out of the following cases occur a. Set to 1 if the SOF is incorrect. It is cleared automatically at receiver start phase. The flag is only valid for 106kbit/s in active or passive communication mode. b. If bit DetectSync in register ModeReg is set to 1 during FeliCa communication or active communication with transfer speeds higher than 106kbit/s, the bit ProtocollErr is set to 1 in case of a length byte violation. c. During the AutoColl command, the bit ProtoCollErr is set to 1, if the Initiator in register ControlReg is set to 1. d. During the MFAuthent command, the bit ProtoCollErr is set to 1, if the number of bytes received in one data stream is incorrect. 5. Set to 1 if the miller decoder detects 2 gaps below the minimum time according to ISO/IEC 1443A definitions.

[1] **Remark:** Command execution will clear all error flags except for bit TempErr. A setting by embedded firmware is impossible.

9.15.18.8 Register Status1

Contains status flags of the CRC, Interrupt and FIFO buffer.

Table 204: CL UART Status1 Register (address DFh or 6337h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CL_interrupt_1	CRCOk	CRCReady	CL_interrupt_0	TRunning	RFOn	HiAlert	LoAlert
Reset	X	0	1	0	0	X	0	1
Access		R	R	R	R	R	R	R

Table 205: Description of CL UART Status1 Register bits

Bit	Symbol	Description
7		This bit shows, if any CL_interrupt_1 source requests attention (with respect to the setting of the interrupt enable flags, see register CommIEnReg and DivIEnReg).
6		Set to 1, the CRC Result is zero. For data transmission and reception the flag CRCOk is undefined (use CRCErr in register ErrorReg). CRCok indicates the status of the CRC co-processor, during calculation the value changes to Zero, when the calculation is done correctly, the value changes to ONE.
5		Set to 1, when the CRC calculation has finished. This flag is only valid for the CRC co-processor calculation.
4		This bit shows, if any CL_interrupt_0 source requests attention (with respect to the setting of the interrupt enable flags, see register CommIEnReg and DivIEnReg).
3		Set to 1, the CLUART timer unit is running, e.g. the timer will decrement the TCounterValReg with the next timer clock. Note: In the gated mode the bit TRunning is set to 1, when the timer is enabled by the register bits. This bit is not influenced by the gated signal.
2		Set to 1, the external RF field is detected.
1		Set to 1, when the number of bytes stored in the FIFO buffer fulfil the following equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ Example: FIFOLength=60, WaterLevel=4 Æ HiAlert =1 FIFOLength=59, WaterLevel=4 Æ HiAlert =0
0		Set to 1, when the number of bytes stored in the FIFO buffer fulfil the following equation: $LoAlert = FIFOLength \leq WaterLevel$ Example: FIFOLength=4, WaterLevel=4 Æ LoAlert =1 FIFOLength=5, WaterLevel=4 Æ LoAlert =0

9.15.18.9 Register Status2

Contain status flags of the receiver, transmitter and data mode detector.

Table 206: CL UART Status2 Register (address E9h or 6338h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TempSenOff	-	RFFreqOK	Target Activated	MF Crypto1 On	ModemState		
Reset	0	X	0	0	0	0	0	0
Access	R/W		R	dy	dy	R	R	R

Table 207: Description of CL UART Status2 Register bits

Bit	Symbol	Description
7	TempSenOff	Set to 1 the internal temperature sensor is switched off.
6	-	Reserved
5	RFFreqOK	Indicates if the frequency detected at the RX pin is in the range of 13.56 MHz. Set to 1, if the frequency at the RX pin is in the range 12 MHz< RX pin frequency<15 MHz. Note: The value of RFFreqOK is not defined if the external RF frequency is in the range of 9 to 12 MHz or in the range of 15 to 19 MHz.
4	Target Activated	Set to 1 if the Select command is received correctly or if the Polling command was answered. Note: This bit can only be set during the AutoColl command in passive communication mode. Note: this bit is cleared automatically by switching off the RF field.
3	MF Crypto1 On	This bit indicates that the MIFARE® Crypto1 unit is switched on and therefore all data communication with the card is encrypted. This bit can only be set to 1 by a successful execution of the MFAuthent Command. This is only valid in reader/writer mode for MIFARE® standard cards.This bit can be cleared by embedded firmware.
2 to 0	ModemState	ModemState shows the state of the transmitter and receiver state machines. Status description: 000 IDLE 001 Wait for StartSend in register BitFramingReg 010 TxWait 011 Transmitting 100 RxWait 101 Wait for data 110 Receiving

9.15.18.10 Register FIFOData

In- and output of 64 bytes FIFO buffer.

Table 208: CL UART FIFOData Register (address EAh or 6339h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData							
Reset	X	X	X	X	X	X	X	X
Access	dy	dy	dy	dy	dy	dy	dy	dy

Table 209: Description of CL UART FIFOData Register bits

Bit	Symbol	Description
7 to 0	FIFOData	Data input and output port for the internal 64 bytes FIFO buffer. The FIFO buffer acts as parallel in/parallel out converter for all data stream in- and outputs

9.15.18.11 Register FIFOLevel

Indicates the number of bytes stored in the FIFO.

Table 210: CL UART FIFOLevel Register (address EBh or 633Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FlushBuffer	FIFOLevel						
Reset	0	0	0	0	0	0	0	0
Access	W	R	R	R	R	R	R	R

Table 211: Description of CL UART FIFOLevel Register bits

Bit	Symbol	Description
7	FlushBuffer	Set to 1, this bit clears the internal FIFO-buffer's read- and write-pointer and the flag BufferOvfl in the register ErrReg immediately. Reading this bit will always return 0.
6 to 0	FIFOLevel	Indicates the number of bytes stored in the FIFO buffer. Writing to the FIFOData Register increments, reading decrements FIFOLevel.

9.15.18.12 Register WaterLevel

Defines the level for FIFO under- and overflow warning.

Table 212: CL UART WaterLevel Register (address ECh or 633Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	WaterLevel					
Reset	X	X	0	0	0	0	0	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 213: Description of CL UART WaterLevel Register bits

Bit	Symbol	Description
7 to 6	-	Reserved.
6 to 0	WaterLevel	This register defines, the warning level of the CLUART for the microcontroller for a FIFO-buffer over- or underflow: The bit HiAlert in Status1Reg is set to 1, if the remaining number of bytes in the FIFO-buffer space is equal or less than the defined WaterLevel bytes.The bit LoAlert in Status1Reg is set to 1, if equal or less than WaterLevel bytes are in the FIFO.

9.15.18.13 Register Control

Diverse Control Register.

Table 214: CL UART WaterLevel Register (address EDh or 633Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow	WrNFCIP-1 ID to FIFO	Initiator	-	RxLastBits		
Reset	X	X	0	0	0	0	0	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 215: Description of CL UART WaterLevel Register bits

Bit	Symbol	Description
7	TStopNow	Set to 1, the timer stops immediately. Reading this bit will always return 0.
6	TStartNow	Set to 1, the timer starts immediately. Reading this bit will always return 0.
5	WrNFCIP-1ID to FIFO	Set to 1, the NFCIP-1ID (10 bytes) is copied into the FIFO. Afterwards the bit is cleared automatically
4	Initiator	Set to 1, The CLUART acts as initiator, otherwise it acts as target.
3	-	Reserved.
2 to 0	RxLastBits	Shows the number of valid bits in the last received byte. If zero, the whole byte is valid.

9.15.18.14 Register BitFraming

Adjustments for bit oriented frames.

Table 216: CL UART BitFraming Register (address EEh or 633Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend	RxAlign			-	TxLastBits		
Reset	0	0	0	0	X	0	0	0
Access	W	dy	dy	dy		dy	dy	dy

Table 217: Description of CL UART BitFraming Register bits

Bit	Symbol	Description
7	StartSend	Set to 1, the transmission of data starts. This bit is only valid in combination with the Transceive command.
6 to 4	RxAlign	Used for reception of bit oriented frames: RxAlign defines the bit position for the first bit received to be stored in the FIFO. Further received bits are stored in the following bit positions. **Example:** RxAlign = 0: The LSB of the received bit is stored at bit 0, the second received bit is stored at bit position 1. RxAlign = 1: The LSB of the received bit is stored at bit 1, the second received bit is stored at bit position 2 RxAlign = 7: The LSB of the received bit is stored at bit 7, the second received bit is stored in the following byte at bit position 0. This flag shall only be used for bitwise anticollision at 106 kbit/s in passive communication mode. In all other modes it shall be set to ZERO.
3	-	Reserved.
2 to 0	TxLastBits	Used for transmission of bit oriented frames: TxLastBits defines the number of bits of the last byte that shall be transmitted. A 000 indicates that all bits of the last byte shall be transmitted.

9.15.18.15 Register Coll

Defines the first bit collision detected on the RF interface.

Table 218: CL UART Coll Register (address EFh or 633Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Values AfterColl	-	CollPos NotValid	CollPos				
Reset	1	X	1	X	X	X	X	X
Access	R/W		R	R	R	R	R	R

Table 219: Description of CL UART Coll Register bits

Bit	Symbol	Description
7	Values AfterColl	If this bit is cleared, all receiving bits will be cleared after a collision.This bit shall only be used during bitwise anticollision at 106 kbit/s, otherwise it shall be set to ONE.
6	-	Reserved.
5	CollPos NotValid	Set to 1, if no Collision is detected or the Position of the Collision is out of range of CollPos. This bit shall only be interpreted in passive communication mode at 106 kbit/s or ISO/IEC 14443A/MIFARE® reader/writer mode.
4 to 0	CollPos	This register shows the bit position of the first detected collision in a received frame, only data bits are interpreted. **Example**: 00h indicates a bit collision in the start bit 01h indicates a bit collision in the 1st bit 08h indicates a bit collision in the 8th bit This bit shall only be interpreted in passive communication mode at 106 kbit/s or ISO/IEC 14443A/MIFARE® reader/writer mode if CollPosNotValid is set to 0.

9.15.18.16 Register SAMClk

Table 220: CL UART SAMClk_en Register (address 6300h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SAMclk_p34_en	-	-	-	Errorbusbitenable	Errorbusbitsel		
Reset	0	X	X	X	0	0	0	0
Access	R/W				R/W	R/W	R/W	R/W

Table 221: Description of CL UART SAMClk_en Register bits

Bit	Symbol	Description
7	SAMclk_p34_en	Set to 1, this bit configures the port P34 to be used as SAMclk. Set to 0, the port P34 is in normal mode
6 to 4	-	Reserved for future use
3	Errorbusbitenable	Set to 1, enable the error source selected by Errorbusbitsel on testbus
2 to 0	Errorbusbitsel	Define the error source on errorbusbit: 00h selects ProtocollErr on testbus 01h selects ParityErr on testbus 02h selects CRCErr on testbus 03h selects CollErr on testbus 04h selects BufferOvfl on testbus 05h selects RFErr on testbus 06h selects TempErr on testbus 07h selects WrErr on testbus

9.15.18.17 Register Mode

Defines general modes for transmitting and receiving.

Table 222: CL UART Mode Register (address 6301h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	DetectSync	TXWaitRF	RxWaitRF	PolSigin	ModeDetOff	CRCPreset	
Reset	0	0	1	1	1	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 223: Description of CL UART Mode Register bits

Bit	Symbol	Description
7	MSBFirst	Set to 1, the CRC co-processor calculates the CRC with MSB first and the CRCResultMSB and the CRCResultLSB in the CRCResultReg registers are bit reversed. Note: During RF communication this bit is ignored.
6	DetectSync	If set to 1, the contactless UART waits for the command F0h before the receiver is activated and F0h is added as a Sync-byte for transmission. This bit is only valid for 106kbit/s during NFCIP-1 data exchange protocol. In all other modes it shall be set to ZERO.
5	TXWaitRF	Set to 1 the transmitter in reader/writer or initiator mode for NFCIP-1 can only be started, if an RF field is generated.
4	RxWaitRF	Set to 1, the counter for RxWait starts only, if an external RF field is detected in target mode for NFCIP-1 or in card communication mode.
3	PolSigin	PolSigin defines the polarity of the SIGIN pin. Set to 1, the polarity of SIGIN pin is active high. Set to 0 the polarity of SIGIN pin is active low. Note: The internal envelope signal is coded active low.
2	ModeDetOff	Set to 1, the internal mode detector is switched off. Note: The mode detector is only active during the AutoColl command.
1 to 0	CRCPreset	Defines the preset value for the CRC co-processor for the command CalCRC. Note: During any communication, the preset values is selected automatically according to the mode definition. 00: 0000 01: 6363 10: A671 11: FFFF

9.15.18.18 Register TxMode

Defines the transmission data rate and framing during transmission.

Table 224: CL UART TxMode Register (address 6302h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TxCRCEn	TxSpeed			InvMod	TxMix	TxFraming	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 225: Description of CL UART TxMode Register bits

Bit	Symbol	Description
7	TxCRCEn	Set to 1, this bit enables the CRC generation during data transmission. Note: This bit shall only set to ZERO at 106kbit/s.
6 to 4	TxSpeed	Defines the bit rate while data transmission. **State:** 000: 106 kbit/s 001: 212 kbit/s 010: 424 kbit/s 011: 848 kbit/s 100: 1696 kbit/s 101: 3392 kbit/s 110: Reserved for future use 111: Reserved for future use
3	InvMod	Set to 1, the modulation for transmitting data is inverted.
2	TxMix	Set to 1, the signal at pin SIGIN is mixed with the internal coder. See Section 9.15.7.4 “Serial Data Switch” on page 132.
1 to 0	TxFraming	Defines the framing used for data transmission. **State:** 00: MIFARE® 01: Active communication mode 10: FeliCa 11: Reserved

9.15.18.19 Register RxMode

Defines the reception data rate and framing during receiving.

Table 226: CL UART RxMode Register (address 6303h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RXCRCEn	RxSpeed			RxNoErr	RxMultiple	RxFraming	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 227: Description of CL UART RxMode Register bits

Bit	Symbol	Description
7	TxCRCEn	Set to 1, this bit enables the CRC generation during reception. Note: This bit shall only set to ZERO at 106 kbit/s.
6 to 4	TxSpeed	Defines the bit rate while data transmission. The contactless analog part handles only transfer speeds up to 424 kbit/s internally, the digital UART handles the higher transfer speed as well. **State:** 000: 106 kbit/s 001: 212 kbit/s 010: 424 kbit/s 011: 848 kbit/s 100: 1696 kbit/s 101: 3392 kbit/s 110: Reserved for future use 111: Reserved for future use
3	InvMod	A not valid received data stream (less than 4 bits received) will be ignored. The receiver will remain active.
2	TxMix	Set to 0, the receiver is deactivated after receiving a data frame. Set to 1, it is possible to receive more than one data frame. This flag is only valid for 212 and 424 kbit/s to handle the Polling command. Having set this bit, the receive and transceive commands will not end automatically. In this the multiple receiving can only be deactivated by writing the IDLE command to the CommandReg register or clearing the bit by the microcontroller. If set to 1, at the end of a received data stream an error byte is added to the FIFO. The error byte is a copy of the ErrorReg register.
1 to 0	TxFraming	Defines the framing used for data transmission. **State:** 00: MIFARE® 01: Active communication mode 10: FeliCa 11: Reserved

9.15.18.20 Register TxControl

Controls the logical behaviour of the antenna driver pins TX1 and TX2.

Table 228: CL UART TxControl Register (address 6304h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	InvTx2RFon	InvTx1RFon	InvTx2RFoff	InvTx1RFoff	Tx2CW	CheckRF	Tx2RFEn	Tx1RFEn
Reset	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W

Table 229: Description of CL UART TxControl Register bits

Bit	Symbol	Description
7	InvTx2RFon	Set to 1, the output signal at pin TX2 will be inverted, if the driver TX2 is enabled.
6	InvTx1RFon	Set to 1, the output signal at pin TX1 will be inverted, if the driver TX1 is enabled.
5	InvTx2RFoff	Set to 1, the output signal at pin TX2 will be inverted, if the driver TX2 is disabled.
4	InvTx1RFoff	Set to 1, the output signal at pin TX1 will be inverted, if the driver TX1 is disabled.
3	Tx2CW	Set to 1, the output signal on pin TX2 will deliver continuously the un-modulated 13.56 MHz energy carrier. Set to 0, TX2Cw is enabled to modulate of the 13.56 MHz energy carrier.
2	CheckRF	Set to 1, Tx2RFEn and Tx1RFEn can not be set if an external RF field is detected.
1	Tx2RFEn	Set to 1, the output signal on pin TX2 will deliver the 13.56 MHz energy carrier modulated by the transmission data.
0	Tx1RFEn	Set to 1, the output signal on pin TX1 will deliver the 13.56 MHz energy carrier modulated by the transmission data.

9.15.18.21 Register TxAuto

Controls the setting of the antenna driver.

Table 230: CL UART TxAuto Register (address 6305h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AutoRFOFF	Force100ASK	AutoWakeUp	-	CAOn	InitialRFOn	Tx2RFAutoEn	Tx1RFAutoEn
Reset	0	0	0	X	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W

Table 231: Description of CL UART TxControl Register bits

Bit	Symbol	Description
7	AutoRFOFF	Set to 1, the antenna driver are switched off after the last data bit has been transmitted as defined in the NFCIP-1 standard. All active drivers are switched off.
6	Force100ASK	Set to 1, Force100ASK forces a 100% ASK Modulation independent of the setting in register ModGsCfgReg.
4	AutoWakeUp	Set to 1, the Contactless module in soft Power-down mode can be waked up by the RF level detector.
3	-	Reserved.
2	InitialRFOn	Set to 1, the collision avoidance is activated and internally the value n is set in accordance to the NFCIP-1 Standard.
2	InitialRFOn	Set to 1, the initial RF collision avoidance is performed and the bit InitialRFOn is cleared afterwards automatically. The bit InitialRFOn will be cleared automatically if the RF is switched on. Note: The driver which should be switched on, have to enabled by bit Tx2RFAutoEn or bit Tx1RFAutoEn.
1	Tx2RFAutoEn	Set to 1, the driver Tx2 is switched on after the external RF field is switched off according to the time TADT. If the bits InitialRFOn and Tx2RFAutoEn are set to 1, Tx2 is switched on if no external RF field is detected during the time TIDT. Note: The times TADT and TIDT are defined in the NFCIP-1P-1 standard.
0	Tx1RFAutoEn	Set to 1, the driver Tx1 is switched on after the external RF field is switched off according to the time TADT. If the bit InitialRFOn and Tx1RFAutoEn are set to 1, Tx1 is switched on if no external RF field is detected during the time TIDT. Note: The times TADT and TIDT are defined in the NFCIP-1P-1 standard.

9.15.18.22 Register TxSel

Selects the internal sources for the analogue part.

Table 232: CL UART TxSel Register (address 6306h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LoadModSel		DriverSel		SigOutSel			
Reset	0	0	0	1				
Access	R/W	R/W	R/W	R/W				

Table 233: Description of CL UART TxSel Register bits

Bit	Symbol	Description
7 to 6	LoadModSel	Selects the input of the LoadMod. **State:** 00: Tristate 01: Modulation signal (envelope) from the internal coder 10: Modulation signal (envelope) from SIGIN 11: Test signal defined by LoadModTest in register TestSel1Reg
5 to 4	DriverSel	Selects the input of driver Tx1 and Tx2. **State:** 00: Tristate Note: In soft power down the driver are only in tristate mode if DriverSel is set to tristate mode. 01: Modulation signal (envelope) from the internal coder 10: Modulation signal (envelope) from SIGIN 11: HIGH Note: The HIGH level depends on the setting of InvTx1RFON/InvTx1RFOff and InvTx2RFON/InvTx2RFOff.
3 to 0	SigOutSel	Selects the input for the SigOut Pin 0000 Tristate 0001 Low 0010 High 0011 TestBus signal as defined by the TestBusBitSel register. 0100 Modulation signal (envelope) from the internal coder 0101 Serial data stream to be transmitted Output signal of the receiver circuit (card modulation signal regenerated and delayed). This signal is used as data output signal for SAM interface connection using 3 lines. Note: To have a valid signal the Contactless uart has to be set to the receving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the Contactless uart in receiving mode. 0111 Serial data stream received as defined by the TestBusBitSel register.

Table 233: Description of CL UART TxSel Register bits *…continued*

Bit	Symbol	Description		
		1000 - 1011	FeliCa Sam modulation	
			1000	RX*
			1001	TX
			1010	Demodulator comparator output
			1011	Reserved
			Note: * To have a valid signal the contactless uart has to be set to the receving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the contactless uart in receiving mode.	
		1100 - 1111	MIFARE Sam modulation	
			1100	RX* with RF carrier
			1101	TX with RF carrier
			1110	RX with RF carrier unfiltered
			1111	RX envelope unfiltered
			Note: *To have a valid signal the contactless uart has to be set to the receving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the contactless uart in receiving mode.	

9.15.18.23 Register RxSel

Selects internal receiver settings.

Table 234: CL UART RxSel Register (address 6307h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UartSel		RxWait					
Reset	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 235: Description of CL UART RxSel Register bits

Bit	Symbol	Description
7 to 6	UartSel	Selects the input of the contactless UART 00: Constant Low 01: Envelope signal at SIGIN 10: Modulation signal from the internal analog part 11: Modulation signal from SIGIN pin. Only valid for transfer speeds above 424 kbit/s
5 to 0	RxWait	After data transmission, the activation of the receiver is delayed for RxWait bit-clocks. During this ‘frame guard time’ any signal at pin Rx is ignored. This parameter is ignored by the receive command. All other commands (e.g. Transceive, Anticoll, Authent) evaluate the parameter. Depending on the mode of the CLUART, the counter starts different. In passive communication mode the counters starts with the last modulation pulse of the previous transmitted data stream. In active communication mode the counter starts immediately after the external RF field is switched on.

9.15.18.24 Register RxTreshhold

Selects thresholds for the bit decoder.

Table 236: CL UART RxTreshhold Register (address 6308h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel				-	Collevel		
Reset	8h	8h	8h	8h	X	4h	4h	4h
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W

Table 237: Description of CL UART RxTreshhold Register bits

Bit	Symbol	Description
7 to 4	MinLevel	Defines the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is not evaluated.
3	-	Reserved.
2 to 0	Collevel	Defines the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester-coded signal to generate a bit-collision relatively to the amplitude of the stronger half-bit.

9.15.18.25 Register Demod

Defines demodulator settings.

Table 238: CL UART Demod Register (address 6309h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AddIQ		FixIQ	-	TauRcv		TauSync	
Reset	1	0	1	X	1	1	0	1
Access			R/W		R/W	R/W	R/W	R/W

Table 239: Description of CL UART Demod Register bits

Bit	Symbol	Description
7 to 6	AddIQ	Defines the use of I and Q channel during reception Note: FixIQ has to be set to 0 to enable the following settings. 00: Select the stronger channel 01: Select the stronger and freeze the selected during communication 10: combines the I and Q channel 11: Reserved for future use
5	FixIQ	If set to 1 and the lower bit of AddIQ is set to 0, the receiving is fixed to I channel. If set to 1 and the lower bit of AddIQ is set to 1, the receiving is fixed to Q channel.
4	-	Reserved.
3 to 2	TauRcv	Changes time-constant of internal PLL during data receiving Note: If set to 0, the PLL is frozen during data receiving.
1 to 0	TauSync	Changes time-constant of internal PLL during burst

9.15.18.26 Register FelNFCIP-11

Defines the length of the FeliCa Sync bytes and the minimum length of the received packet.

Table 240: CL UART FelNFCIP-11 Register (address 630Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FelSyncLen		DataLenMin					
Reset	1	0	1	X	1	1	0	1
Access			R/W		R/W	R/W	R/W	R/W

Table 241: Description of CL UART FelNFCIP-11 Register bits

Bit	Symbol	Description
7 to 6	FelSyncLen	Defines the the length of the Sync bytes. **State:** 00: B2 4D 01: 00 B2 4D 10: 00 00 B2 4D 11: 00 00 00 B2 4D
5 to 0	DataLenMin	This bit defines the minimum length of the accepted packet length: DataLenMin*4<= data packet length. This parameter is ignored at 106 kbit/s if the bit DetectSync in register ModeReg is set to 0. If a received package is shorter as the defined DataLenMin value, the package will be ignored.

9.15.18.27 Register FelNFCIP-12

Defines the maximum length of the received packet.

Table 242: CL UART FelNFCIP-12 Register (address 630Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WaitForSelected	ShortTimeSlot	DataLenMax					
Reset	X	0	0	0	0	0	0	0
Access			R/W	R/W	R/W	R/W	R/W	R/W

Table 243: Description of CL UART FelNFCIP-12 Register bits

Bit	Symbol	Description
7	WaitForSelected	Set to 1, the AutoColl command is automatically quilted only, if: 1. A valid select procedure according to ISO/IEC 14443A has been performed. 2. A valid command is received after a valid polling procedure according to the FeliCa specification. Note: If this bit is set, no active communication is possible.Note: Setting this bit reduces the CPU interaction in case of a communication to a second device in the same RF field during passive communication mode.
6	ShortTimeSlot	Defines the timeslot length for active communication mode at 424 kbit/s. Set to 1 a short time slot is used (half of the timeslot at 212 kbit/s). Set to 0 a long timeslot is used (similaras the timeslot for 212 kbit/s).
5 to 0	DataLenMax	This bit defines the maximum length of the accepted packet length: DataLenMax*4 > data packet length Note: If set to ZERO the maximum data length is 256 bytes. This parameter is ignored at 106 kbit/s if the bit DetectSync in register ModeReg is set to 0.If a received package is larger as the defined DataLenMax value, the package will be ignored.

9.15.18.28 Register MifNFCIP-1

Defines ISO/IEC 14443A / MIFARE® / NFCIP-1 specific settings in target or card operating mode.

Table 244: CL UART MifNFCIP-1 Register (address 630Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SensMiller			TauMiller		MFHalted	TxWait	
Reset	0	1	1	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 245: Description of CL UART MifNFCIP-1 Register bits

Bit	Symbol	Description
7 to 5	SensMiller	This bit defines the sensitivity of the Miller decoder.
4 to 3	TauMiller	This bit defines the time constant of the Miller decoder.
2	MFHalted	Set to 1, this bit indicates that the contactless UART is set to HALT mode in card interface mode at 106 kbit/s. This bit has to be set by the microcontroller and indicates that only the code 52h is accepted as a request command. This bit is cleared automatically by RF reset.
1 to 0	TxWait	This bit defines the additional response time for the target at 106 kbit/s in passive communication mode and during the AutoColl command. Per default 7 bits are added to the value of the register bit.

9.15.18.29 Register ManualRCV

Allows manual fine tuning of the internal receiver.

IMPORTANT NOTE: For standard application it is not recommended to change this register settings.

Table 246: CL UART ManualRCV Register (address 630Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	Parity Disable	LargeBWPLL	ManualHPCF	HPCF	
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

Table 247: Description of CL UART ManualRCV Register bits

Bit	Symbol	Description
7 to 5	-	Reserved, for Future Use.
4	Parity Disable	Set to 1, parity check is disabled.
3	LargeBWPLL	Set to 1, the bandwidth of the internal PLL for clock recovery is extended.
2	ManualHPCF	Set to 0, the HPCF bits are ignored and the HPCF settings are adapted automatically to the receiving mode.
1 to 0	HPCF	Selects the High Pass Corner Frequency (HPCF) of the filter in the internal receiver chain 00 For signals with frequency spectrum down to 106 kHz 01 For signals with frequency spectrum down to 212 kHz 10 For signals with frequency spectrum down to 424 kHz 11 For signals with frequency spectrum down to 848 kHz

9.15.18.30 Register CRCResultMSB

Shows the actual MSB values of the CRC calculation.

Table 248: CL UART CRCResultMSB Register (address 6311h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultMSB							
Reset	FFh	FFh	FFh	FFh	FFh	FFh	FFh	FFh
Access	R	R	R	R	R	R	R	R

Table 249: Description of CL UART CRCResultMSB Register bits

Bit	Symbol	Description
7 to 0	CRCResultMSB	This register shows the actual value of the most significant byte of the CRC register. It is valid only if bit CRC Ready in register Status1 is set to 1.

9.15.18.31 Register CRCResultLSB

Shows the actual LSB values of the CRC calculation.

Table 250: CL UART CRCResultLSB Register (address 6312h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultLSB							
Reset	FFh	FFh	FFh	FFh	FFh	FFh	FFh	FFh
Access	R	R	R	R	R	R	R	R

Table 251: Description of CL UART CRCResultLSB Register bits

Bit	Symbol	Description
7 to 0	CRCResultLSB	This register shows the actual value of the most significant byte of the CRC register. It is valid only if bit CRC Ready in register Status1 is set to 1.

9.15.18.32 Register GsNLoadMod

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when there is no RF generated by the PN531.

Table 252: CL UART GsNLoadMod Register (address 6313h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CWGsNLoadMod				ModGsNLoadMod			
Reset	8h	8h	8h	8h	8h	8h	8h	8h
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 253: Description of CL UART GsNLoadMod Register bits

Bit	Symbol	Description
7 to 4	CWGsNLoadMod	The value of this register defines the conductance of the output N-driver when there is no RF generated by the PN531. This may be used to regulate the output power and subsequently current consumption and operating distance. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1.
3 to 0	ModGsNLoadMod	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1.

9.15.18.33 Register ModWidth

Controls the setting of the modulation width.

Table 254: CL UART ModWidth Register (address 6314h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidth							
Reset	26h	26h	26h	26h	26h	26h	26h	26h
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 255: Description of CL UART ModWidth Register bits

Bit	Symbol	Description
7 to 0	ModWidth	These bits define the width of the Miller modulation as initiator in active and passive communication mode as multiples of the carrier frequency (ModWidth+1 / fc). The maximum value is half the bit period. Acting as a target in passive communication mode at 106 kbit/s or in card interface mode for ISO/IEC 14443A / MIFARE® these bits are used to change the duty cycle of the subcarrier frequency. The resulting number of carrier periods for LOW value is calculated #clocksLOW=(ModWidth modulo 8)+1. For the HIGH value: #clocksHIGH=16-#clocksLOW.

9.15.18.34 Register TxBitPhase

Adjust the TX bitphase at 106 kbit/s.

Table 256: CL UART TxBitPhase Register

Bit	Name	Description	Reset	R/W
7	RcvClkChange	Set to 1, the demodulator's clock is derivated by the external RF field.	1	R/W
6:0	TxBitPhase	These bits are representing the number of carrier frequency clock cycles, which are added to the waiting period before transmitting data in all communication modes. TXBitPhase is used to adjust the TX bit synchronization during passive NFCIP-1 communication mode at 106 kbit/s and in ISO/IEC 14443A / MIFARE® reader/writer mode.	07h	R/W

Table 257: CL UART TxBitPhase Register (address 6315h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RcvClkChange	TxBitPhase						
Reset	1	07h	07h	07h	07h	07h	07h	07h
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 258: Description of CL UART TxBitPhase Register bits

Bit	Symbol	Description
7	RcvClkChange	Set to 1, the demodulator's clock is derivated by the external RF field.
6 to 0	TxBitPhase	These bits are representing the number of carrier frequency clock cycles, which are added to the waiting period before transmitting data in all communication modes. TXBitPhase is used to adjust the TX bit synchronization during passive NFCIP-1 communication mode at 106 kbit/s and in ISO/IEC 14443A / MIFARE® reader/writer mode.

9.15.18.35 Register RFCfg (6316h)

Configures the receiver gain and RF level.

Table 259: CL UART RFCfg Register

Bit	Name	Description	Reset	R/W
7	RFLevelAmp	Set to 1, this bit activates the RF level detectors' amplifier.	0	R/W
6:4	RxGain	This register defines the receivers signal voltage gain factor: State: 000: 18dB 001: 23 dB 010: 18 dB 011: 23 dB 100: 33 dB 101: 38 dB 110: 43 dB 111: 48 dB	100	R/W
3:0	RFLevel	Defines the sensitivity of the RF level detector, for description see Section 9.15.7.2 "RF level detector" on page 131.	1000	R/W

9.15.18.36 Register GsN (6317h)

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2.

Table 260: CL UART GsN Register

Bit	Name	Description	Reset	R/W
7:4	CWGsN	The value of this register defines the conductance of the output N-driver. This may be used to regulate the output power and subsequently current consumption and operating distance. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1.	8h	R/W
3:0	ModGsN	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1.	8h	R/W

9.15.18.37 Register CWGsP (6318h)

Defines the conductance of the P-driver.

Table 261: CL UART CWGsP Register

Bit	Name	Description	Reset	R/W
7:6	-	Reserved	x	
5:0	CWGsP	The value of this register defines the conductance of the output P-driver. This may be used to regulate the output power and subsequently current consumption and operating distance. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1.	20h	R/W

9.15.18.38 Register ModGsP (6319h)

Defines the driver P-output conductance for the time of modulation.

Table 262: CL UART ModGsP Register

Bit	Name	Description	Reset	R/W
7:6	-	Reserved	x	
5:0	ModGsP	The value of this register defines the conductance of the output P-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1.	20h	R/W

9.15.18.39 Register TMode (631Ah)

Defines settings for the internal timer.
Note: This register is splitted into 2 8bit register.

Table 263: CL UART TMode Register

Bit	Name	Description	Reset	R/W
7	TAuto	Set to 1, the timer starts automatically at the end of the transmission in passive communication mode or when an external RF field is detected. The timer stops immediately after receiving the first data bit if the bit RxMultiple in the register RxModeReg is not set. If RxMultiple is set to 1, the timer never stops. In this case the timer can be stopped by setting the bit TStopNow in register ControlReg to 1. Set to 0 indicates, that the timer is not influenced by the protocol.	0	R/W
6:5	TGated	The internal timer is running in gated mode. Note: In the gated mode, the bit TRunning is 1 when the timer is enabled by the register bits. This bit does not influence the gating signal 00: No gated mode 01: gated by SIGIN 10 Gated by AUX1 11: Reserved	00	R/W
4	TAutoRestart	Set to 1, the timer automatically restart its count-down from TReloadValue, instead of counting down to zero. Set to 0 the timer decrements to zero and the bit TimerIRq is set to 1.	0	R/W
3:0	TPrescaler_Hi	Defines higher 4 bits for TPrescaler. The following formula is used to calculate f_{Timer}: $f_{Timer} = 6.78\ MHz / ^{TPreScaler}$. For detailed description see Section 9.15.12.1 “Timer” on page 140.	0000	R/W

9.15.18.40 Register TPrescaler (631Bh)

Define the LSB of the Timer-Prescaler.

Table 264: CL UART TPrescaler Register

Bit	Name	Description	Reset	R/W
7:0	TPrescaler_LO	Defines lower 8 bits for TPrescaler. The following formula is used to calculate f_{Time}: $f_{Timer} = 6.78\ MHz / ^{TPreScaler}$. For detailed description see Section 9.15.12.1 “Timer” on page 140.	00	R/W

9.15.18.41 Register TReload_hi (631Ch)

Defines the MSB of the 16 bit long timer reload value.

Table 265: CL UART TReloadVal_hi Register

Bit	Name	Description	Reset	R/W
7:0	TReloadVal_Hi	Defines the higher 8 bits for the TReloadReg. With a start event the timer loads with the TReloadValue. Changing this register affects the timer only with the next start event.	00h	R/W

9.15.18.42 Register TReload_lo (631Dh)

Defines the LSB of the 16 bit long timer reload value.

Table 266: CL UART TReload_lo Register

Bit	Name	Description	Reset	R/W
7:0	TReloadVal_Lo	Defines the lower 8 bits for the TReloadReg. With a start event the timer loads with the TReloadValue. Changing this register affects the timer only with the next start event.	XXh	R/W

9.15.18.43 Register TCounterVal_hi (631Eh)

Defines the MSB byte of the current value of the timer.

Table 267: CL UART TCounterVal_hi Register

Bit	Name	Description	Reset	R/W
7:0	TCounterVal_Hi	MSB of the current value of the timer (Higher 8 bits).	XXh	R

9.15.18.44 Register TCounterVal_lo (631Fh)

Defines the LSB byte of the current value of the timer.

Table 268: CL UART TCounterVal_lo Register

Bit	Name	Description	Reset	R/W
7:0	TCounterVal_LO	LSB of the current value of the timer (Lower 8 bits).	XXh	R

9.15.18.45 Register TestSel1 (6321h)

General test signal configuration.

Table 269: CL UART TestSel1 Register

Bit	Name	Description	Reset	R/W
7:6	LoadModTst	Defines the test signal for the LOADMOD pin Note: The bits LoadModSel in register TXSelReg has to be set to 11 to enable LoadModTst: 00: Low 01: high 10: Reserved for future use 11: TstBusBit as defined by the TestBusBitSel register	00	R/W
5:4	Samclksel	Defines the source for the 13.56 MHz SAM clock 00: GND - SAM clock is switched off 01: Clock derivated by the internal oscillator 10: Internal UART clock 11: Clock derivated by the RF Field	00	R/W
3	SAMClkD1	Set to 1, the SAM clock is delivered to P31 if the observe_cluart bit is set to 1.	0	R/W
2:0	TstBusBitSel	Select the TstBusBit from the testbus.	000	R/W

9.15.18.46 Register TestSel2 (6322h)

General testsignal configuration and PRBS control.

Table 270: CL UART TestSel2 Register

Bit	Name	Description	Reset	R/W
7	TstBusFlip	If set to 1, the internal testbus(D6-D0) is mapped to the parallel port by the following order: D4,D3, D2,D6,D5, D0, D1.	x	R/W
6	PRBS9	Starts and enables the PRBS9 sequence according ITU-TO150. Note: All relevant register to transmit data have to be configured before entering PRBS9 mode. Note: The data transmission of the defined sequence is started by the send command.	0	R/W
5	PRBS15	Starts and enables the PRBS15 sequence according ITU-TO150. Note: All relevant register to transmit data have to be configured before entering PRBS15 mode. Note: The data transmission of the defined sequence is started by the send command.	0	R/W
4:0	TstBusSel	Selects the testbus source. See Section 9.15.16.2 “Testbus” on page 147.	00000	R/W

9.15.18.47 Register TestPinValue (6324h)

Defines the values for the 7 bit parallel port when it is used as I/O

Table 271: CL UART TestPinValue Register

Bit	Name	Description	Reset	R/W
7	useio	Set to 1, define that the TestPinValue is transferred to the testbus	0	R/W
6:0	TestPinValue	Defines the value of the testbus, when useio is set to 1.	00h	R/W

9.15.18.48 Register TestBus (6325h)

Shows the status of the internal testbus.

Table 272: CL UART TestBus Register

Bit	Name	Description	Reset	R/W
7:0	TestBus	Shows the status of the internal testbus. The testbus is selected by the register TestSel2. See Section 9.15.16.2 “Testbus” on page 147	0	R

9.15.18.49 Register Autotest (6326h)

Controls the digital selftest.

Table 273: CL UART Autotest Register

Bit	Name	Description	Reset	R/W
7	-	Reserved	0	R
6	AmpRcv	Set to 1 the internal signal processing in the receiver chain is performed non-linear. This increases the operating distance in communication modes at 106 kbit/s. Note: Due to non linearity the effect of min- and coll level are as well non linear.	1	R
5:4	-	Reserved	00	R
3:0	SelfTest	Enables the digital self test. The selftest can be started by the selftest command in the command register. The selftest is enabled by 1001. Note: For default operation the selftest has to be disabled (0000).	0000	R/W

9.15.18.50 Register Version (6327h)

Shows the version of the contactless UART.

Table 274: CL UART Version Register

Bit	Name	Description	Reset	R/W
7:0	Version	24h indicates contactless module Version V0. 25h indicates contactless module Version V0.1. 26h indicates contactless module Version V0.2.	XXh	R

9.15.18.51 Register AnalogTest (6328h)

Controls the pins AUX1 and AUX2.

Table 275: CL UART AnalogTest Register

Bit	Name	Description		Reset	R/W
7:4	AnalogSelAux1	Controls the AUX1 pin. Note: All testsignals are described in Section 9.15.16.3 “Testsignals at pin AUX” on page 147.		XXh	R
		0000	Tristate		
		0001	Output of TestDAC1 (AUX1), output of TESTDAC2 (AUX2) Note: Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.		
		0010	Testsignal Corr1 Note: Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.		
		0011	0011 Testsignal Corr2 Note: Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.		
		0100	Testsignal MinLevel Note: Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.		
		0101	ADC channel I Note: Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.		

Table 275: CL UART AnalogTest Register

Bit	Name	Description		Reset	R/W
		0110	ADC channel Q Note: Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.		
		0111	ADC channel I combined with Q Note: Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.		
		1000	Signal for production test Note: Current output. The use of 1 kΩ pull down resistor on AUX1 is recommended.		
		1001	SAM clock (13.56 MHz)		
		1010	HIGH		
		1011	LOW		
		1100	TxActive At 106 kbit /s: HIGH during Startbit, Data bit, Parity and CRC. At 212 and 424 kbit: High during Preamble, Sync, Data and CRC		
		1101	RxActive At 106 kbit /s: HIGH during Data bit, Parity and CRC. At 212 and 424 kbit: High during Data and CRC		
		1110	Subcarrier detected At 106 kbit /s: not applicable. At 212 and 424 kbit: High during last part of Preamble, Sync, Data and CRC		
		1111	testbusbit as defined by the TestBusSel register		
3:0	AnalogSelAux2	Controls the AUX2 pin. Note: All testsignals are described in Section 9.15.16.3 “Testsignals at pin AUX” on page 147.		XXh	R
		0000	Tristate		
		0001	Output of TestDAC1 (AUX1), output of TESTDAC2 (AUX2) Note: Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.		
		0010	Testsignal Corr1 Note: Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.		
		0011	0011 Testsignal Corr2 Note: Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.		
		0100	Testsignal MinLevel Note: Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.		
		0101	ADC channel I Note: Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.		
		0110	ADC channel Q Note: Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.		

Table 275: CL UART AnalogTest Register

Bit	Name	Description		Reset	R/W
		0111	ADC channel I combined with Q Note: Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.		
		1000	Signal for production test Note: Current output. The use of 1 kΩ pull down resistor on AUX2 is recommended.		
		1001	SAM clock (13.56 MHz)		
		1010	HIGH		
		1011	LOW		
		1100	TxActive At 106 kbit /s: HIGH during Startbit, Data bit, Parity and CRC. At 212 and 424 kbit: High during Preamble, Sync, Data and CRC		
		1101	RxActive At 106 kbit /s: HIGH during Data bit, Parity and CRC. At 212 and 424 kbit: High during Data and CRC		
		1110	Subcarrier detected At 106 kbit /s: not applicable. At 212 and 424 kbit: High during last part of Preamble, Sync, Data and CRC		
		1111	testbusbit as defined by the TestBusSel register		

9.15.18.52 Register TestDAC1 (6329h)

Defines the testvalue for TestDAC1.

Table 276: CL UART TestDAC1 Register

Bit	Name	Description	Reset	R/W
7:6	-	Reserved	XX	R
5:0	TestDAC1	Defines the testvalue for TestDAC1. The output of the DAC1 can be switched to AUX1 by setting AnalogSelAux1 to 0001.	XXh	R/W

9.15.18.53 Register TestDAC2 (632Ah)

Defines the testvalue for TestDAC2.

Table 277: CL UART TestDAC2 Register

Bit	Name	Description	Reset	R/W
7:6	-	Reserved	XX	R
5:0	TestDAC2	Defines the testvalue for TestDAC2. The output of the DAC2 can be switched to AUX2 by setting AnalogSelAux2 to 0001.	XXh	R/W

9.15.18.54 Register TestADC (632Bh)

Shows the actual value of ADC I and Q channel.

Table 278: CL UART TestADC Register

Bit	Name	Description	Reset	R/W
7:4	ADC_I	Shows the actual value of ADC I channel.	Xh	R
3:0	ADC_Q	Shows the actual value of ADC Q channel.	Xh	R

10. Limiting values

Table 279: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
PVDD, SVDD, TVDD, AVDD, DVDD	Supply Voltages		-0.5	4	V
VBUS	USB Supply Voltage		-0.5	5.5	V
P_{totusb}	Total power dissipation in USB mode			550	mW
P_{tot}	Total power dissipation (VBUS and DVDD in short cut mode)			150	mW
I_{TX1}	Maximum current in transmitter TX1		-100	100	mA
I_{TX2}	Maximum current in transmitter TX2		-100	100	mA
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature			125	°C

Table 280: ESD Characteristics

Symbol	Parameter	Conditions	Specification	Value
ESDH	ESD Susceptibility (Human Body model)	1500 Ohm, 100pF	JESD22-A114-B	2 KV
ESDM	ESD Susceptibility (Machine model)	0.75 µH, 200 pF	JESD22-A114-A	200 V
ESDC	ESD Susceptibility (Charge Device model)	Field induced model	JESC22-C101-A	1 KV

11. Recommended operating conditions

Table 281: Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Tamb	Ambient Temperature			-30	+25	+85	°C
VBUS	USB Supply Voltage (USB mode)	VSS = 0V	[1]	4.2	5	5.25	V
	Supply Voltage (Non USB mode)	VBUS=DVDD VSS = 0V		2.5	3.3	3.6	V

Table 281: Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TVDD, AVDD, DVDD	Supply Voltages	TVDD=AVDD=DVDD VSS = 0V	[2] [3]	2.5	3.3	3.6	V
PVDD	Supply Voltage for host interface	VSS = 0V		1.6	1.8 - 3.3	3.6	V
SVDD	Output Voltage for SAM	VSS = 0V Sam_switch_en set to 1		DV_{DD} -0.1	3.3	DV_{DD}	V

[1] VSS represents DVSS, TVSS1, TVSS2, AVSS.

[2] AVDD, DVDD and TVDD shall always be on the same voltage level.

[3] Supply voltage of AVDD, DVDD and TVDD below 3 V reduces the performance (e.g. the achievable operating distance).

12. Thermal characteristics

Table 282: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{thj-a}	thermal resistance from junction to ambient (for HVQFN40 package)	in free air with exposed pad soldered on a 4 layer Jedec PCB-0.5		37	41.1	K/W

13. Characteristics

Table 283: Voltage regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBUS	USB Supply Voltage (USB mode)	VSS = 0V	4.2	5	5.25	V
DVDD	Supply voltage after Inrush current limitation (USB mode)	From IDVDD=0 to IDVDD= 150mA	2.95	3.3	3.6	V
IVBUS	Maximum load current (USB mode)	measured on VBUS			150	mA
	Maximum Inrush current limitation	At power up (curlimoff =0)			100	mA
Vth1	Threshold voltage on DVDD falling			2.4		V
Vhys1	Hysteresis on Vth1		40	60	100	mV
Cdec	Decoupling capacitor on DVDD		10			mF

[1] The internal regulator is only enabled when the USB interface is selected by I0 and I1.

Table 284: Current Consumption

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Ihpd	Hard Power Down Current (Not powered from USB)	AVDD=DVDD=TVDD= PVDD=3V, RF level detector off	[5]		5	10	mA
ISPD	Soft Power down Current (Not powered from USB)	AVDD=DVDD=TVDD= PVDD=3V, SVDD=0V, RF level detector on	[5]		18	30	mA
Isupend	USB suspend Current	VBUS=5V, AVDD=DVDD=TVDD= PVDD=3V, SVDD=0V, RF level detector on (without resistor on D+/D-)	[5]		120	250	mA
IDVDD	Digital Supply Current	AVDD=DVDD=TVDD= PVDD=3V, RF level detector on			12		mA
IAVDD	Analog Supply Current	AVDD=DVDD=TVDD= PVDD=3V, RF level detector on			1.5	6	mA
IAVDDrcvoff	Analog Supply Current	AVDD=DVDD=TVDD= PVDD=3V, RF level detector off			3	5	mA
IPVDD	Pad Supply Current		[2]			30	mA
ISVDD	Output Supply Current for SAM	sam_switch_en set to 1	[3]			30	mA
ITVDD1,4	Transmitter Supply Current	Continuous Wave, TVDD=3V	[1] [4]		602	100	mA

[1] ITVDD depends on TVDD and the external circuitry connected to Tx1 and Tx2.

[2] IPVDD depends on the overall load at the digital pins.

[3] ISVDD depends on the overall load on SVDD pad.

[4] During operation with a typical circuitry the overall current is below 100 mA.

[5] ISPD and IHPD are the total currents over all supplies.

[6] Typical value using a complementary driver configuration and an antenna matched to 40 Ohm between TX1 and TX2 at 13.56 MHz.

13.1 Input Pin characteristics for RSTPD

Table 285: Input Pin characteristics for RSTPD

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage			PVDD - 0.4		PVDD	V
VIL	Low level Input voltage			0		0.4	V
IIH	High level input current	Vi=PVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA
Cin	Input Capacitance				2.5		pF

13.2 Input Pin characteristics for I0, I1 and TESTEN

Table 286: Input Pin characteristics for I0, I1 and TESTEN

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*DVDD		DVDD	V
VIL	Low level Input voltage		[2]	0		0.3*DVDD	V
IIH	High level input current	Vi=DVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA
ILeak	Input Leakage current	RSTPD=DVDD		-1		1	mA
Cin	Input Capacitance				2.5		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is DVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

13.3 Input/output Pin characteristics for P35

Table 287: Input/output Pin characteristics for P35

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*DVDD		DVDD	V
VIL	Low level Input voltage		[2]	0		0.3*DVDD	V
VOH	High level output voltage	DVDD=3V, IOH=-4mA		DVDD - 0.4		DVDD	V
VOL	Low level output voltage	DVDD=3V, IOL=4mA		0		0.4	V
IOH	High level output current	DVDD=3V, VOH=DVDD - 0.4	[3]	-4			mA
IOL	Low level output current	DVDD=3V, VOL=0.4		4			mA
IIH	High level input current	Vi=DVDD				1	mA
IIL	Low level input current	Vi=0V				50	mA
		Vi=DVDD/2				1	mA
ILeak	Input leakage current	RSTPD=DVDD		-1		1	mA
Cin	Input Capacitance				2.5		pF
Cout	Max Load				30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is DVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

[3] Only valid during tpushpull time as defined for quasi bidirectional pads Figure 23 "Quasi Bidirectional".

13.4 Output Pin characteristics for RSTOUT

Table 288: Output Pin characteristics for RSTOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH	High level output voltage	PVDD=3V, IOH=-4mA	0.7*PVDD		PVDD	V
		PVDD=1.8V, IOH=-2mA	0.7*PVDD		PVDD	V
VOL	Low level output voltage	PVDD=3V, IOL=4mA	0		0.3*PVDD	V
		PVDD=1.8V, IOL=2mA	0		0.3*PVDD	V

Table 288: Output Pin characteristics for RSTOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOH	High level output current	PVDD=3V, VOH=0.8*PVDD	-4			mA
		PVDD=1.8V, VOH=0.7*PVDD	-2			mA
IOL	Low level output current	PVDD=3V, VOL=0.2*PVDD	4			mA
		PVDD=3V, VOL=0.3*PVDD	2			mA
Cout	Max Load			30		pF

13.5 Input/Output Pin characteristics for IRQ

Table 289: Input/Output Pin characteristics for IRQ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*PVDD		PVDD	V
VIL	Low level Input voltage		[2]	0		0.3*PVDD	V
VOH	High level output voltage	PVDD=3V, IOH=-4mA		0.7*PVDD		PVDD	V
		PVDD=1.8V, IOH=-2mA		0.7*PVDD		PVDD	V
VOL	Low level output voltage	PVDD=3V, IOL=4mA		0		0.3*PVDD	V
		PVDD=1.8V, IOL=2mA		0		0.3*PVDD	V
IOH	High level output current	PVDD=3V, VOH=0.8*PVDD	[3]	-4			mA
		PVDD=1.8V, VOH=0.7*PVDD		-2			mA
IOL	Low level output current	PVDD=3V, VOL=0.2*PVDD		4			mA
		PVDD=3V, VOL=0.3*PVDD		2			mA
IIH	High level input current	Vi=DVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA
ILeak	Input leakage current	RSTPD=PVDD		-1		1	mA
Cin	Input Capacitance				2.5		pF
Cout	Max Load				30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is PVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

[3] Only valid during tpushpull time as defined for quasi bidirectional pads Figure 23 "Quasi Bidirectional".

13.6 Input/Output Pin characteristics for P30, P31, P32_INT0, P33_INT1

Table 290: Input/Output Pin characteristics for P30, P31, P32_INT0, P33_INT1

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*PVDD		PVDD	V
VIL	Low level Input voltage		[2]	0		0.3*PVDD	V

Table 290: Input/Output Pin characteristics for P30, P31, P32_INT0, P33_INT1

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VOH	High level output voltage	PVDD=3V, IOH=-4mA		PVDD-0.4		PVDD	V
		PVDD=1.8V, IOH=-2mA		PVDD-0.4		PVDD	V
VOL	Low level output voltage	PVDD=3V, IOL=4mA		0		0.4	V
		PVDD=1.8V, IOL=2mA		0		0.4	V
IOH	High level output current	PVDD=3V, VOH=0.8*PVDD	[3]	-4			mA
		PVDD=1.8V, VOH=0.7*PVDD		-2			mA
IOL	Low level output current	PVDD=3V, VOL=0.2*PVDD		4			mA
		PVDD=3V, VOL=0.3*PVDD		2			mA
IIH	High level input current	Vi=DVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA
ILeak	Input leakage current	RSTPD=PVDD		-1		1	mA
Cin	Input Capacitance				2.5		pF
Cout	Max Load				30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is PVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

[3] Only valid during tpushpull time as defined for quasi bidirectional pads Figure 23 "Quasi Bidirectional".

13.7 Input Pin characteristics for NSS

Table 291: Input Pin characteristics for NSS for HSU / SPI interfaces

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*PVDD		PVDD	V
VIL	Low level Input voltage		[2]	0		0.3*PVDD	V
IIH	High level input current	Vi=DVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA
ILeak	Input leakage current	RSTPD=PVDD		-1		1	mA
Cin	Input Capacitance				2.5		pF
Cout	Max Load				30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is PVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

Table 292: Input/open drain output Pin characteristics for NSS for I^2C interface

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*PVDD		PVDD	V
VIL	Low level Input voltage		[2]	0		0.3*PVDD	V
VOL	Low level output voltage	PVDD=3V, IOL=4mA		0		0.3	V
		PVDD=1.8V, IOL=2mA		0		0.3	V

Table 292: Input/open drain output Pin characteristics for NSS for I^2C interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOL	Low level output current	PVDD=3V, VOL=0.3*PVDD	3			mA
		PVDD=3V, VOL=0.3*PVDD	2			mA
IIH	High level input current	Vi=DVDD			1	mA
IIL	Low level input current	Vi=0V			1	mA
ILeak	Input leakage current	RSTPD=PVDD	-1		1	mA
Cin	Input Capacitance			2.5		pF
Cout	Max Load			30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is PVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

Table 293: Input/Output Pin characteristics for NSS for USB interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level Input voltage	PVDD=3V	2		3.6	V
VIL	Low level Input voltage	[1]	0		0.8	V
VOH	High level output voltage	PVDD=3V, RPD=15 kΩ to VSS	2.8		PVDD	V
VOL	Low level output voltage	PVDD=3V, RPU=1.5 kΩ to PVDD	0		0.3	V
IIH	High level input current	Vi=DVDD			1	mA
IIL	Low level input current	Vi=0V			1	mA
ILeak	Input leakage current	RSTPD=PVDD	-1		1	mA
Cin	Input Capacitance			2.5		pF
Cout	Max Load			30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

13.8 Input/Output Pin characteristics for MOSI

Table 294: Input/Output Pin characteristics for MOSI for HSU and SPI Interfaces

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High level Input voltage	[1]	0.7*PVDD		PVDD	V
VIL	Low level Input voltage	[2]	0		0.3*PVDD	V
VOH	High level output voltage	PVDD=3V, IOH=-4mA	PVDD-0.4		PVDD	V
		PVDD=1.8V, IOH=-2mA	PVDD-0.4		PVDD	V
VOL	Low level output voltage	PVDD=3V, IOL=3mA	0		0.3	V
IOH	High level output current	PVDD=3V, VOH=0.8*PVDD [3]	-3			mA
		PVDD=1.8V, VOH=0.7*PVDD	-2			mA

Table 294: Input/Output Pin characteristics for MOSI for HSU and SPI Interfaces

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOL	Low level output current	PVDD=3V, VOL=0.2*PVDD	3			mA
		PVDD=3V, VOL=0.3*PVDD	2			mA
IIH	High level input current	Vi=DVDD			1	mA
IIL	Low level input current	Vi=0V			1	mA
ILeak	Input leakage current	RSTPD=PVDD	-1		1	mA
Cin	Input Capacitance			2.5		pF
Cout	Max Load			30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is PVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

[3] Only valid during tpushpull time as defined for quasi bidirectional pads Figure 23 "Quasi Bidirectional".

Table 295: Input/open drain output Pin characteristics for MOSI for I²C interface

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*PVDD		PVDD	V
VIL	Low level Input voltage		[2]	0		0.3*PVDD	V
VOL	Low level output voltage	PVDD=3V, IOL=4mA		0		0.3	V
		PVDD=1.8V, IOL=2mA		0		0.3	V
IOL	Low level output current	PVDD=3V, VOL=0.3*PVDD		3			mA
		PVDD=3V, VOL=0.3*PVDD		2			mA
IIH	High level input current	Vi=DVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA
ILeak	Input leakage current	RSTPD=PVDD		-1		1	mA
Cin	Input Capacitance				2.5		pF
Cout	Max Load				30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is PVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

Table 296: Input/Output Pin characteristics for MOSI for USB interface

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage	PVDD=3V		2		3.6	V
VIL	Low level Input voltage		[1]	0		0.8	V
VOH	High level output voltage	PVDD=3V, RPD=15 kΩ to VSS		2.8		PVDD	V
VOL	Low level output voltage	PVDD=3V, RPU=1.5 kΩ to PVDD		0		0.3	V
IIH	High level input current	Vi=DVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA

Table 296: Input/Output Pin characteristics for MOSI for USB interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ILeak	Input leakage current	RSTPD=PVDD	-1		1	mA
Cin	Input Capacitance			2.5		pF
Cout	Max Load			30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

13.9 Input/Output Pin characteristics for MISO/ SCK

Table 297: Input/Output Pin characteristics for MISO/ SCK

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*PVDD		PVDD	V
VIL	Low level Input voltage		[2]	0		0.3*PVDD	V
VOH	High level output voltage	PVDD=3V, IOH=-4mA		PVDD-0.4		PVDD	V
		PVDD=1.8V, IOH=-2mA		PVDD-0.4		PVDD	V
VOL	Low level output voltage	PVDD=3V, IOL=4mA		0		0.4	V
		PVDD=1.8V, IOL=2mA		0		0.4	V
IOH	High level output current	PVDD=3V, VOH=0.8*PVDD	[3]	-4			mA
		PVDD=1.8V, VOH=0.7*PVDD		-2			mA
IOL	Low level output current	PVDD=3V, VOL=0.2*PVDD		4			mA
		PVDD=3V, VOL=0.3*PVDD		2			mA
IIH	High level input current	Vi=DVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA
ILeak	Input leakage current	RSTPD=PVDD		-1		1	mA
Cin	Input Capacitance				2.5		pF
Cout	Max Load				30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is PVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

[3] Only valid during tpushpull time as defined for quasi bidirectional pads Figure 23 "Quasi Bidirectional".

13.10 Output Pin characteristics for Delatt

Table 298: Output Pin characteristics for delatt

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VOH	High level output voltage	PVDD=3V, IOH=-2mA	[1]	0.8*PVDD		PVDD	V
IOZ	Tristate output leakage current	When switched off				10	mA

[1] Optional connection for an external 1.5K resistor on D+.

13.11 Input Pin characteristics for SIGIN

Table 299: Input/Output Pin characteristics for MISO/ SCK

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*SVDD		SVDD	V
VIL	Low level Input voltage		[2]	0		0.3*SVDD	V
IIH	High level input current	Vi=SVDD				1	mA
IIL	Low level input current	Vi=0V				1	mA
ILeak	Input leakage current	RSTPD=PVDD		-1		1	mA
Cin	Input Capacitance				2.5		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is SVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

13.12 Output Pin characteristics for SIGOUT

Table 300: Output Pin characteristics for SIGOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH	High level output voltage	DV_{DD} -0.1 < SV_{DD} < DV_{DD}, IOH = -4 mA	SVDD-0.4		SVDD	V
VOL	Low level output voltage	DV_{DD} -0.1 < SV_{DD} < DV_{DD}, IOL = +4 mA	0		0.4	V
IOH	High level output current	SVDD=3V, VOH=0.8*SVDD	-4			mA
IOL	Low level output current	SVDD=3V, VOL=0.2*SVDD	4			mA
		SVDD=3V, VOL=0.3*SVDD	2			mA
ILeak	Input leakage current	RSTPD=PVDD	-1		1	mA
Cin	Input Capacitance			2.5		pF
Cout	Max Load			30		pF

13.13 Input/Output Pin characteristics for P34

Table 301: Input/Output Pin characteristics for P34

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VIH	High level Input voltage		[1]	0.7*SVDD		SVDD	V
VIL	Low level Input voltage		[2]	0		0.3*SVDD	V
VOH	High level output voltage	SVDD=3V, IOH=-4mA		SVDD-0.4		SVDD	V
VOL	Low level output voltage	SVDD=3V, IOL=4mA		0		0.4	V
IOH	High level output current	SVDD=3V, VOH=0.8*SVDD	[3]	-4			mA
IOL	Low level output current	SVDD=3V, VOL=0.2*SVDD		4			mA
		SVDD=3V, VOL=0.3*SVDD		2			mA
IIH	High level input current	Vi=SVDD				1	mA

Table 301: Input/Output Pin characteristics for P34

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IIL	Low level input current	Vi=0V			1	mA
ILeak	Input leakage current	RSTPD=PVDD	-1		1	mA
Cin	Input Capacitance			2.5		pF
Cout	Max Load			30		pF

[1] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is SVDD - 0.4 Volts.

[2] The value doesn't guaranty the power-down consumptions. To reach the specified power-down consumptions, the limit is 0.4 Volt.

[3] Only valid when configured in Figure 25 "Push/Pull Output" or during tpushpull time as defined for quasi bidirectional pads Figure 23 "Quasi Bidirectional".

13.14 Output Pin characteristics for LOADMOD

Table 302: Output Pin characteristics for LOADMOD

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VOH	High level output voltage	DVDD=3V, IOH=-4mA		DVDD-0.4		DVDD	V
VOL	Low level output voltage	DVDD=3V, IOL=4mA		0		0.4	V
IOH	High level output current	DVDD=3V, VOH=0.8*DVDD	[3]	-4			mA
IOL	Low level output current	DVDD=3V, VOL=0.2*DVDD		4			mA
ILeak	Input leakage current	RSTPD=PVDD		-1		1	mA
Cout	Max Load				10		pF

13.15 Input Pin characteristics for RX

Table 303: Input Pin characteristics for RX

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VINRX	Dynamic Input voltage Range	AVDD=3V	-1		AVDD+1	V
Cinrx	RX Input Capacitance			10		pF
Rinrx	RX Input Series resistance	AVDD = 3V, Receiver active, VRX = 1Vpp, 1.5 V DC offset		350		Ohm
VRX,MinIV, Mill	Minimum Input voltage, Miller coded	AVDD = 3V, 106 kbit/s		150		mVpp
VRX,MinIV, Man	Minimum Input voltage, Manchester Coded	AVDD = 3V, 212 and 424 kbit/s		100		mVpp
VRX,MaxIV, Mill	Maximum Input voltage, Miller coded	AVDD = 3V, 106 kbit/s		4		Vpp

Table 303: Input Pin characteristics for RX

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRX,MaxIV, Man	Maximum Input voltage, Manchester Coded	AVDD = 3V, 212 and 424 kbit/s		4		Vpp
mRX,Mill	Minimum Modulation index, Miller coded	AVDD = 3V,106kbit/s VRX=1.5Vpp, SensMiller = 3		33		%
VRXMod,Man	Minimum modulation voltage	AVDD = 3V, RxGain= 7		5		mV

[1] The minimum modulation voltage is valid for all modulation schemes except Miller coded signals.

[2] The Figure 56 “RX Voltage definitions” outlines the voltage definitions.

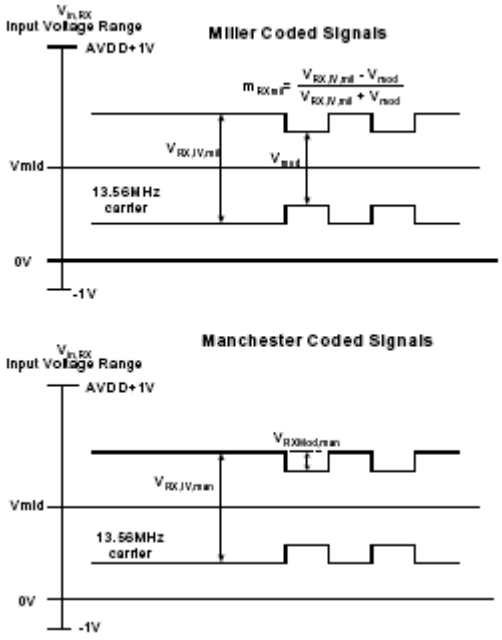


Fig 56. RX Voltage definitions

13.16 Pin characteristics for 27.12 MHz XTAL Oscillator (OSCIN, OSCOUT)

Table 304: Pin characteristics for 27.12 MHz XTAL Oscillator (OSCIN, OSCOUT)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ILeakOSCIN	Input Leakage current	RSTPD=PVDD	-1		1	mA
VIHOSCIN	High level Input voltage		0.7*AVDD		AVDD	V
VILOSCIN	Low level Input voltage		0		0.3*AVDD	V
DCOSCIN	DC input voltage			0.650		V
CinOSCIN	OSCIN Input Capacitance	AVDD=2.8V, VDC=0.65V, VAC=1Vpp		1		pF
VOHOSCOUT	High level output voltage			1.1		V

Table 304: Pin characteristics for 27.12 MHz XTAL Oscillator (OSCIN, OSCOUT)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOLOSCOUT	Low level output voltage			0.2		V
CinOSCOUT	Input Capacitance			1		pF
fOSCIN	Clock Frequency	with an appropriate x-tal		27.12 ±7 kHz		MHz
DFEC	Duty Cycle of Clock Frequency		49.5	50	50.5	%

13.17 Pin characteristics for 4 MHz XTAL Oscillator (OSCIN, OSCOUT)

Table 305: Pin characteristics for 4 MHz XTAL Oscillator (OSCIN, OSCOUT)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ILeakOSCIN	Input Leakage current	RSTPD=PVDD	-1		1	mA
VIHOSCIN	High level Input voltage		0.7*DVDD		DVDD	V
VILOSCIN	Low level Input voltage		0		0.3*DVDD	V
DCOSCIN	DC input voltage			DVDD/2		V
CinOSCIN	OSCIN Input Capacitance	AVDD=2.8V, VDC=0.65V, VAC=1Vpp		1.0		pF
VOHOSCOUT	High level output voltage				0.3DVDD	V
VOLOSCOUT	Low level output voltage		0			V
CinOSCOUT	Input Capacitance			1.0		pF
fOSCIN	Clock Frequency	with an appropriate x-tal		4		MHz
DFEC	Duty Cycle of Clock Frequency		45	50	55	%

13.18 Output Pin characteristics for AUX1/AUX2

Table 306: Output Pin characteristics for AUX1/AUX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH	High level output voltage	DVDD=3V, IOH=-4mA	DVDD-0.4		DVDD	V
VOL	Low level output voltage	DVDD=3V, IOL=4mA	DVSS		DVSS+0.4	V
IOH	High level output current	DVDD=3V, VOH=DVDD-0.3	-4			mA
IOL	Low level output current	DVDD=3V, VOL=0.3	4			mA
ILeak	Input leakage current	RSTPD=PVDD	-1		1	mA
Cin	Input Capacitance			2.5		pF
Cout	Max Load			15		pF

13.19 Output Pin characteristics for TX1/TX2

Table 307: Output Pin characteristics for TX1/TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOH,C32,3 V	High level output voltage	TVDD=3V and ITX =32mA, CWGsP=3F(Hex)	TVDD-150			mV
VOH,C80,3 V	High level output voltage	TVDD= 3V and ITX = 80mA,CWGsP=3F(Hex)	TVDD-400			mV
VOH,C32,2 V5	High level output voltage	TVDD=2.5V and ITX =32mA,CWGsP=3F(Hex)	TVDD-240			mV
VOH,C80,2 V5	High level output voltage	TVDD=2.5V and ITX =80 mA,CWGsP=3F(Hex)	TVDD-640			mV
VOL,C32,3 V	Low level output voltage	TVDD=3V and ITX =32mA, CWGsN=F(Hex)			150	mV
VOL,C80,3 V	Low level output voltage	TVDD= 3V and ITX = 80mA,CWGsN=F(Hex)			400	mV
VOL,C32,2 V5	Low level output voltage	TVDD=2.5V and ITX =32mA,CWGsN=F(Hex)			240	mV
VOL,C80,2 V5	Low level output voltage	TVDD=2.5V and ITX =80 mA,CWGsN=F(Hex)			640	mV

14. Dynamic characteristics

14.1 Timing for Reset

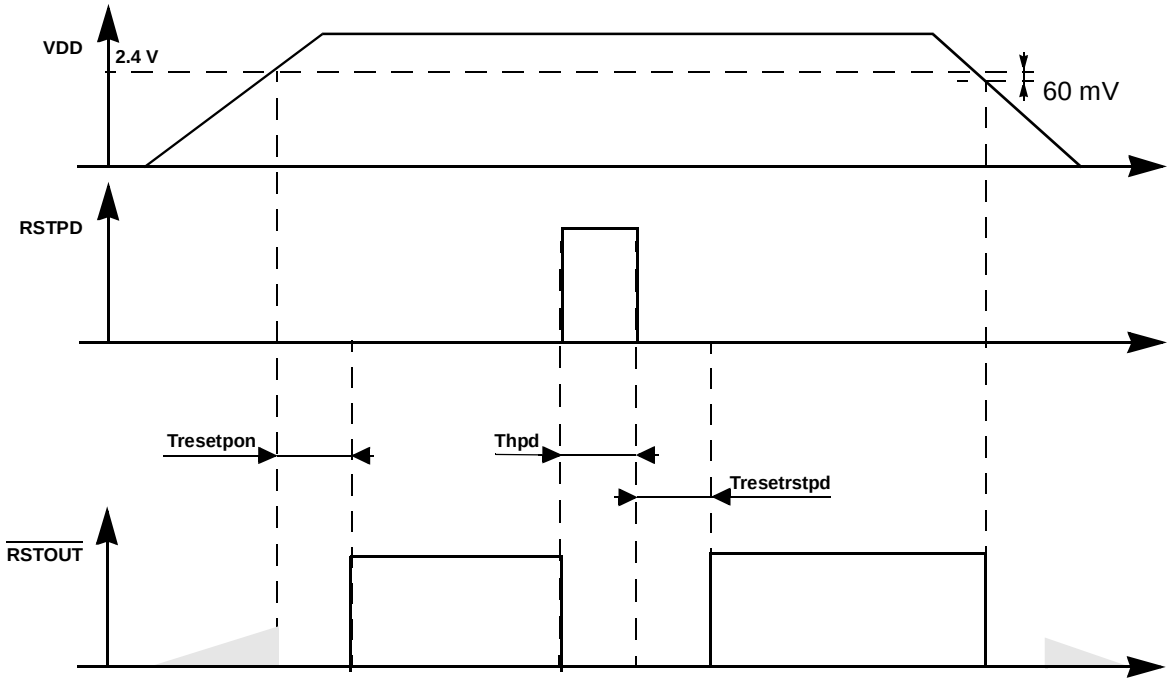


Fig 57. System reset overview

Table 308: Reset Duration Time

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Tresetpon	Reset time at power on		[1]	0.1	0.4	2	ms
Thpd	Hard power-down time	User dependent		20			ns
Tresetrstpd	Reset time when RSTPD is released		[1]	0.1	0.4	2	ms

[1] Depends on the 27.12 MHz crystal oscillator startup time.

14.2 Timing for the SPI compatible interface

Table 309: SPI timing specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tSCKL	SCK low pulse width		50			ns
tSCKH	SCK high pulse width		50			ns
tSHDX	SCK high to data changes		25			ns
tDXSH	data changes to SCK high		25			ns
tSLDX	SCK low to data changes				25	ns
tSLNH	SCK low to NSS high		0			ns

[1] The signal NSS has to be low to be able to send several bytes in one datastream.

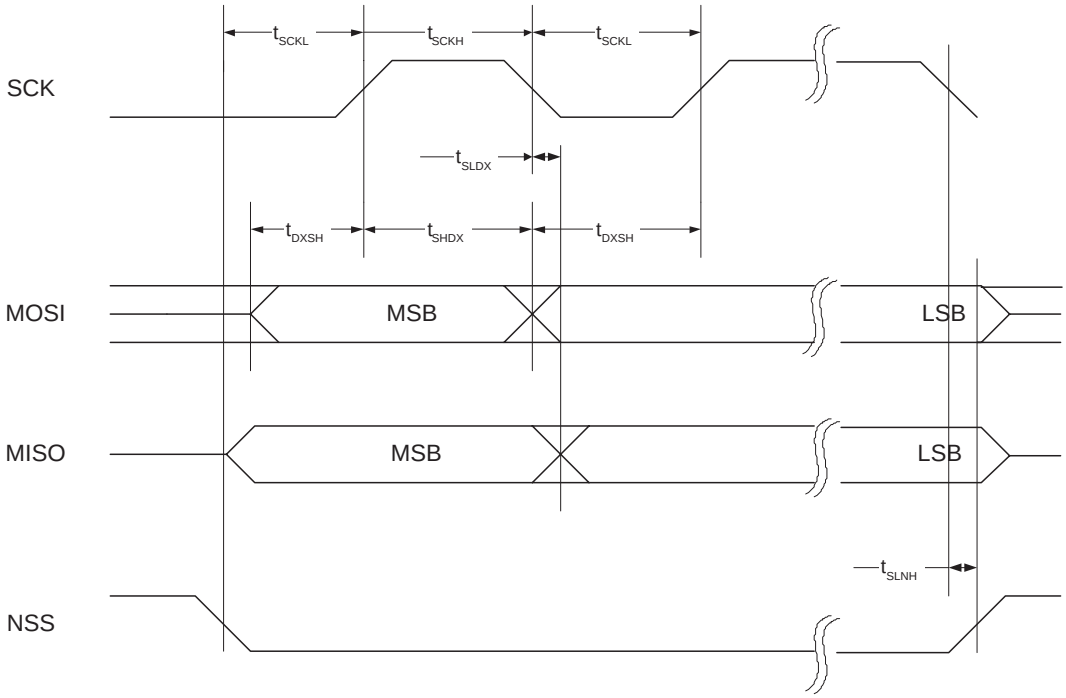


Fig 58. SPI timing diagram

14.3 Timing for the I²C interface

Table 310: I²C timing specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fSCL	SCL clock frequency		0		400	kHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated		600			ns
tSU;STA	Set-up time for a repeated START condition		600			ns
tSU;STO	Set-up time for STOP condition		600			ns
tLOW	LOW period of the SCL clock		1300			ns
tHIGH	HIGH period of the SCL clock		600			ns
tHD;DAT	Data hold time			900		ns
tSU;DAT	Data set-up time		100			ns
trscl	Rise time SCL signals		20	300		ns
tfscl	Fall time SCL signals		20	300		ns

Table 310: I²C timing specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
trsda	Rise time of both SDA and SCL signals		20	300		ns
tfsda	Fall time of both SDA and SCL signals		20	300		ns
tBUF	Bus free time between a STOP and START condition		1.3			ms

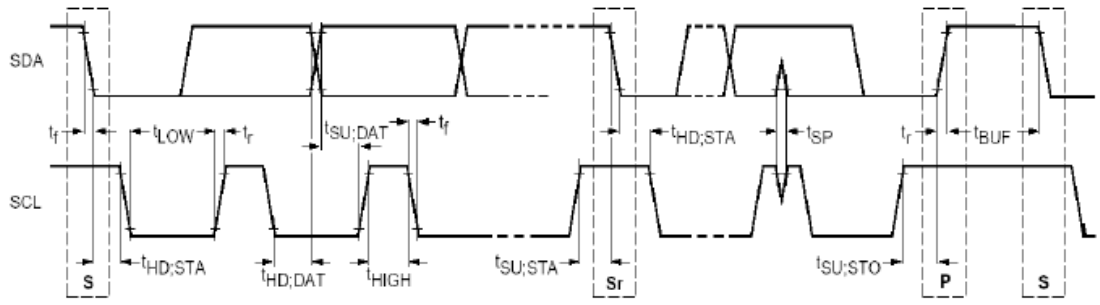


Fig 59. I²C timing diagram

15. Application information

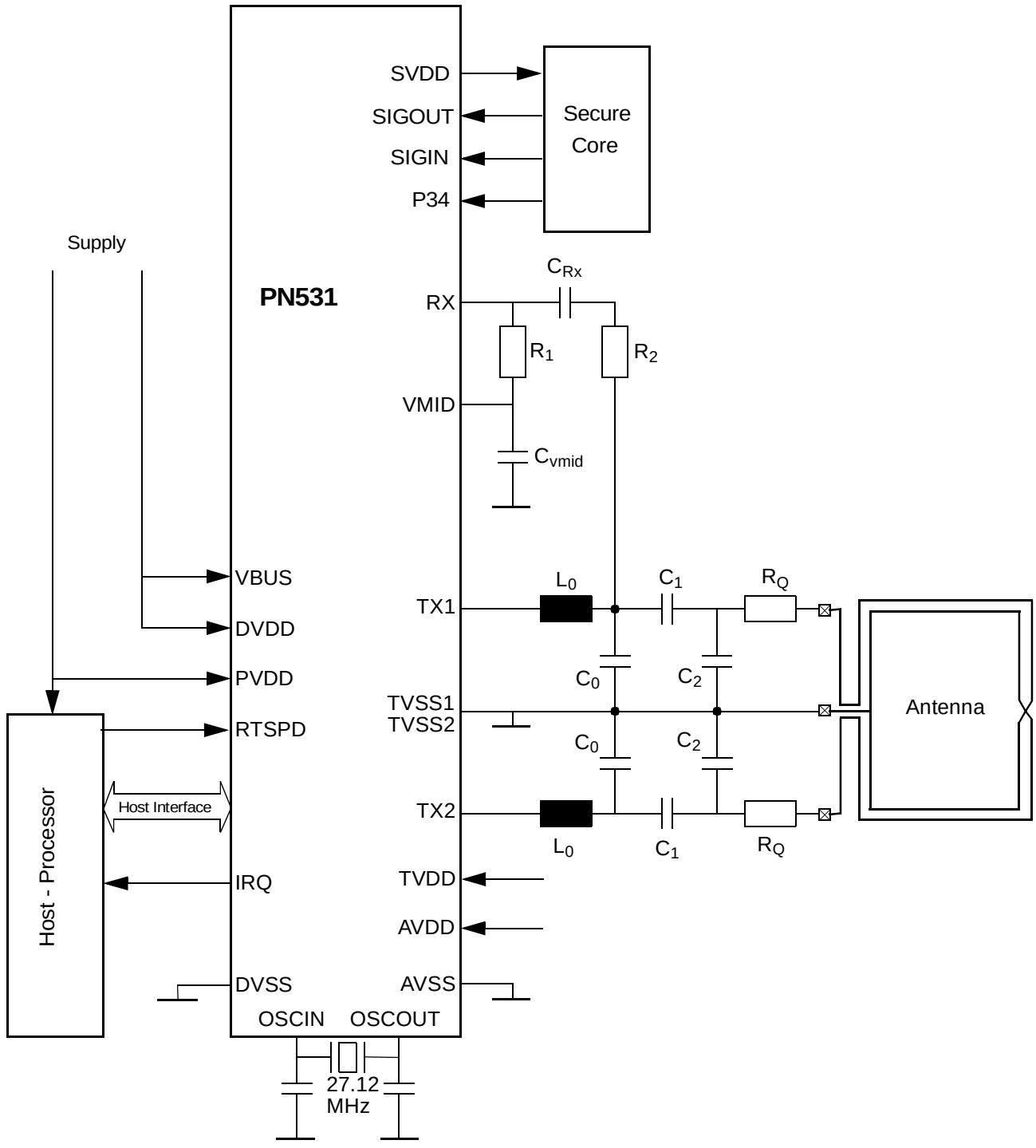
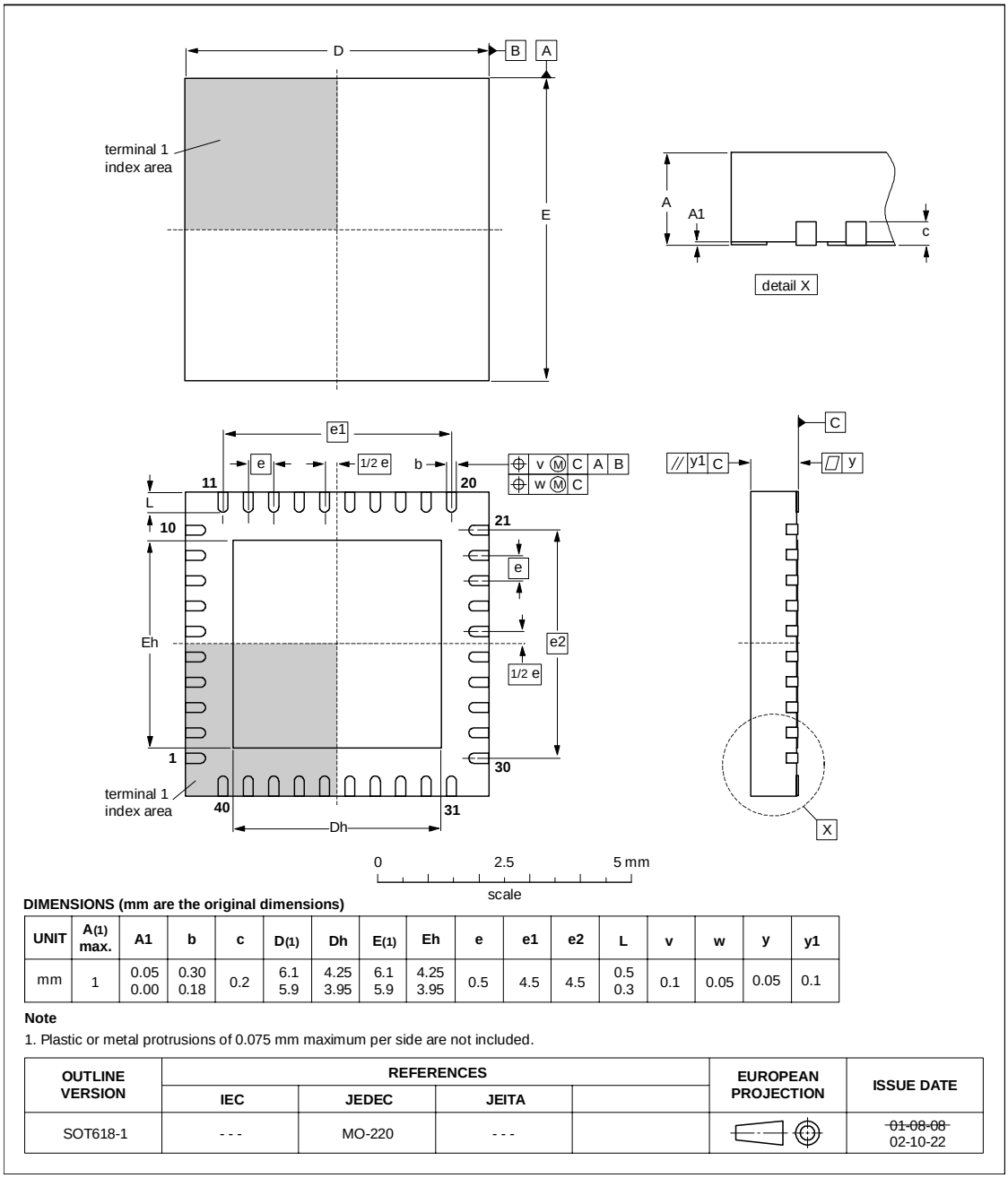


Fig 60. Application diagram of PN531

16. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT618-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 61. Package outline HVQFN40 (SOT618-1)

17. Abbreviations

Table 311: Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
PCD	Proximity Coupling Device. Definition for a Card Reader/ Writer according to the ISO/IEC 14443 Specification
PICC	Proximity Cards. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443A/ MIFARE®
PICC -> PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443A/ MIFARE®
Initiator	Generates RF field @ 13.56 MHz and starts the NFCIP-1 communication.
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin) / (Vmax + Vmin).
Loadmodulation Index	The load modulation index is defined as the card's voltage ratio (Vmax - Vmin) / (Vmax + Vmin) measured at the card's coil.
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).

18. Revision history

Table 312: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
		Product data sheet			
Modifications:	• Initial version				

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19. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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